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HIGH PERMITTIVITY DIELECTRICS FOR NEXT GENERATIONS OF INTEGRATED CIRCUITS

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High permittivity dielectrics for next generations of integrated circuits

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A thesis submitted in partial fulfillment of the requirements for the degree of Doctor by

Pedro Carlos Feijoo Guerro

A mi padre, José Luis,
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TABLE OF CONTENTS

ABSTRACT

This thesis studies two different approaches for further downscaling in the CMOS technology and the flash memory devices. In the first place, we study $Gd_{2-x}Sc_xO_3$ deposited by high pressure sputtering as a candidate for the third generation of high κ dielectrics. We studied the high κ material/Si interface, and an optimization of the growing conditions of the binary components (Gd_2O_3 and Sc_2O_3). We assessed the influence of the metal gate on the properties of the binary oxides, comparing Al (reactive), Pt (noble metal) and Ti (oxygen scavenger). Then, we grew ~8 nm amorphous Gd-rich $Gd_{2-x}Sc_xO_3$ films by alternating nano-laminates of Gd_2O_3 and Sc_2O_3. Pt gated metal-insulator-semiconductor devices show low density of interface defects, capacitance-voltage hysteresis and leakage current. $Gd_{2-x}Sc_xO_3$ also presents better thermal stability than its binary components. An outstanding value of 25 was calculated for the relative effective permittivity, which makes $Gd_{2-x}Sc_xO_3$ a promising choice for the third generation of high κ dielectrics. On the other hand, we studied the reliability of ultra low equivalent oxide thickness triple gated MISFET devices. Three-dimensional transistor architectures are currently replacing traditional planar MISFETs, so the assessment of the reliability becomes vital. Time-dependent dielectric breakdown and positive bias temperature instabilities in FinFETs present no major differences with their planar counterparts.

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

Acronym	Meaning
ALD	atomic layer deposition
BD	breakdown
BE	binding energy
BTI	bias temperature instabilities
CMOS	complementary metal-oxide-semiconductor
CMP	chemical mechanical polishing
CP	charge pumping
CVD	chemical vapor deposition
CVS	constant voltage stress
DI	deionized
ECR	electron cyclotron resonance
EOT	equivalent oxide thickness
FGA	forming gas anneal
FIB	focused ion beam
FinFET	fin field effect transistor
FTIR	Fourier transform infrared spectroscopy
GDOS	glow discharge optical spectroscopy
GIXRD	glancing incidence x-ray diffraction
HBD	hard breakdown
HF	high frequency
HP	high performance
HPS	high pressure sputtering
IC	integrated circuit
IL	interlayer
ITRS	International Technology Roadmap for Semiconductors
LOP	low operating voltage
MFC	mass flow controller
MIS	metal-insulator-semiconductor
MISFET	metal-insulator-semiconductor field effect transistor
MOCVD	metal-organic chemical vapor deposition
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field effect transistor

Acronym	Meaning
MUGFET	multiple gate field effect transistor
NBTI	negative bias temperature instabilities
PBTI	positive bias temperature instabilities
PECVD	plasma enhanced chemical vapor deposition
PLD	pulsed laser deposition
RCA	Radio Corporation of America
rf	radio frequency
SBD	soft breakdown
SC	standard clean
SIMS	secondary ion mass spectroscopy
SMR	selective material removal
SOI	silicon on insulator
TDDB	time-dependent dielectric breakdown
TEM	transmission electron microscopy
TOF	time of flight
XPS	X-ray photoelectron spectroscopy

LIST OF SYMBOLS

Symbol	Unit (SI)	Description
A	m^2	area
A	adim.	absorbance in FTIR
B	-	constant in PBTI
C	$F\ m^{-2}$	capacitance per unit area
C	-	constant in PBTI
c	$m\ s^{-1}$	light speed ($3.0\times10^8\ m\ s^{-1}$)
C_B	F	matching capacitance
C_{HF}	$F\ m^{-2}$	high frequency capacitance per unit area
C_{ins}	$F\ m^{-2}$	insulator capacitance per unit area
C_{it}	$F\ m^{-2}$	capacitance per unit area due to interface defects
C_m	$F\ m^{-2}$	measured capacitance per unit area
$C_{m,cor}$	$F\ m^{-2}$	corrected capacitance per unit area
C_{ma}	$F\ m^{-2}$	measured capacitance per unit area in strong accumulation
C_{QS}	$F\ m^{-2}$	quasi static capacitance per unit area
D	-	constant in PBTI
d_{hkl}	m	distance between planes of Miller indexes *hkl*
D_{it}	$J^{-1}\ m^{-2}$	density of interface defects
ΔQ	C	displacement charge
E	J	photon energy
E_b	J	binding energy
E_C	J	conduction band
E_g	J	energy band gap
E_i	J	intrinsic level
E_{ip}	$V\ m^{-1}$	incident electric field (component parallel to incidence plane)
E_{is}	$V\ m^{-1}$	incident electric field (component perpendicular to incidence plane)
E_K	J	kinetic energy
EOT	m	equivalent oxide thickness
E_{rp}	$V\ m^{-1}$	reflected electric field (component parallel to incidence plane)
E_{rs}	$V\ m^{-1}$	reflected electric field (component perpendicular to incidence plane)
E_V	J	valence band

Symbol	Unit (SI)	Description
f	Hz	frequency
F	adim.	cumulative distribution function
F_{hkl}	adim.	structure factor
G_{m}	S m^{-2}	measured conductance per unit area
$G_{\mathrm{m,cor}}$	S m^{-2}	corrected conductance per unit area
G_{ma}	S m^{-2}	measured conductance per unit area in strong accumulation
G_{P}	S m^{-2}	parallel conductance per unit area
h	J s	Planck constant (6.6×10^{-34} J s)
H_{fin}	m	fin height
i	adim.	number of failed device
i	-	imaginary unit
I	W	resultant light intensity in FTIR
I_0	W	initial light intensity in FTIR
I_{cp}	A	charge pumping current
I_{G}	A	gate leakage current
I_{t}	W	transmitted light intensity in FTIR
J_{G}	A m^{-2}	gate leakage current density
k_{B}	J K^{-1}	Boltzmann constant
L_{D}	m	Debye length
L_{ext}	m	fin extension
L_{G}	m	gate length
m	adim.	coefficient of interaction
N	adim.	number of tested device
n	adim.	refrative index
n	adim.	integer number
N_{A}	m^{-3}	acceptor impurity density
N_{D}	m^{-3}	donor impurity density
N_{fin}	adim.	number of fins.
n_{i}	m^{-3}	intrinsic number of carrier
N_{it}	adim.	Total number of defects in the dielectric
$N_{\mathrm{it\|SW}}$	m^{-2}	density of defects in the sidewall
$N_{\mathrm{it\|TW}}$	m^{-2}	density of defects in the top-wall
q	C	elementary charge (1.6×10^{-19} C)

Symbol	Unit (SI)	Description
Q_G	C m^{-2}	charge at the metal gate
Q_{it}	C m^{-2}	charge trapped in the interface defects
Q_{sc}	C m^{-2}	charge density in the semiconductor
Q_{ss}	C m^{-2}	charge density in the insulator/semiconductor interface
r	m	distance
R_p	adim.	Fresnel coefficient (perpendicular component)
R_S	Ω m^2	series resistance
R_s	adim.	Fresnel coefficient (parallel component)
S	m	pitch (distance between fins)
T	K	temperature
t	s	time
T	adim.	transmission coefficient in FTIR
$t_{0.01\%}$	s	final lifetime extrapolation at 0.01% failures
t_{BD}	s	time to breakdown
T_c	K	critic temperature for superconductors
t_{HBD}	s	time to hard breakdown
t_{IL}	m	thickness of the interfacial layer
t_{ins}	m	thickness of the high κ-insulator
t_{LF}	s	lifetime
t_{SBD}	s	time to soft breakdown
t_{stress}	s	stress time in PBTI
V	V	voltage
V_D	V	drain voltage
V_{FB}	V	flatband voltage
V_G	V	gate voltage
V_{ins}	V	voltage drop at the insulator
V_{ins0}	V	voltage drop at the insulator when V_G =0
V_{sense}	V	sense voltage in PBTI
V_{stress}	V	stress voltage in PBTI
V_{TH}	V	threshold voltage
W_{fin}	m	fin width
x	m	displacement
Y_m	S m^{-2}	measured admittance

Symbol	Unit (SI)	Description
z	adim.	Weibull parameter
α	adim.	constant in PBTI
β	adim.	Weibull slope
χ_{i}	V	insulator electron affinity
χ_{sc}	V	semiconductor electron affinity
Δ	adim.	phase difference in ellipsometry
ε_0	F m^{-1}	permittivity of vacuum (8.85×10^{-12} F m^{-1})
ε_{ins}	F m^{-1}	permittivity of the insulator
ε_S	F m^{-1}	permittivity of the semiconductor
ϕ_F	V	difference between semiconductor work function and intrinsic level
ϕ_m	V	metal work function
ϕ_{ms}	V	metal-semiconductor work function difference
ϕ_{sc}	V	semiconductor work function
γ	adim.	acceleration factor in TDDB
η	s	time to 63% failures
κ	adim.	relative permittivity
κ_{eff}	adim.	effective relative permittivity of the dielectric stack
κ_{GdO}	adim.	relative permittivity of gadolinium oxide
κ_{IL}	adim.	relative permittivity of the interface layer
κ_{ins}	adim.	relative permittivity of the high κ insulator
κ_{ScO}	adim.	relative permittivity of scandium oxide
κ_{SiN}	adim.	relative permittivity of silicon oxide (~8)
κ_{SiO}	adim.	relative permittivity of silicon oxide (3.9)
λ	m	wavelength
ν	m^{-1}	wavenumber
ν	s^{-1}	photon frequency
θ	rad	half the angle that X-ray source and detector make
θ_{hkl}	rad	diffraction angle corresponding to plane of Miller indexes *hkl*
υ	adim.	constant in PBTI
ω	rad s^{-1}	angular frequency
ω	rad	the angle that X-ray source and sample make
ψ	adim.	amplitude component in ellipsometry

Symbol	Unit (SI)	Description
ψ_S	V	voltage drop at the semiconductor surface
ψ_{S0}	V	voltage drop at the semiconductor surface when V_G =0

SUMMARY

The complementary metal-oxide-semiconductor (CMOS) integrated circuit technology based on silicon (Si) has dominated the microelectronics industry since the late 80s. This has been possible thanks to the continuous reduction of the dimensions of the main active device: the metal-insulator-semiconductor field-effect transistor (MISFET). One of the key enablers of the downscaling of the MISFET was the dielectric used in the isolation between the metal gate (highly doped poly-crystalline Si or poly-Si) and the channel in the semiconductor (Si): the silicon oxide (SiO_2). In fact, this device has been traditionally named MOSFET, since the insulator is the silicon substrate oxide. In 2008, SiO_2 was replaced by a high permittivity dielectric (high κ dielectric), a hafnium-based dielectric, to overcome critical problems in the downscaling of silicon devices. Current research is focused on new strategies for the next generations of MISFETs, such as new high κ materials or new device fabrication routes.

The main objective of this thesis is to study two different approaches to continue with the downscaling of MISFET. In the first place, a third generation of gate dielectrics –scandium oxide (Sc_2O_3), gadolinium oxide (Gd_2O_3) and gadolinium scandate ($Gd_{2-x}Sc_xO_3$)- is investigated. Also, different metal gates –aluminum (Al, reactive), titanium (Ti, oxygen scavenger) and platinum (Pt, non-reacting)- are studied for their integration with the high κ dielectrics. Secondly, a new device architecture is characterized, the fin-based field effect transistor (FinFET), which is a three-dimensional transistor whose channel is folded instead of being planar.

This thesis proposes high pressure sputtering (HPS) for the deposition of Sc_2O_3, Gd_2O_3 and $Gd_{2-x}Sc_xO_3$. In this nonconventional sputtering, the working pressure is around 1 mbar, between two and three orders of magnitude higher than typical sputtering systems. The high pressure shortens the mean free path of the processing gas up to 50 μm. The sputtered and reflected particles from the target thermalize within a short distance (1-3 mm), through gas collisions. The thermalization length is much shorter than the target-substrate distance (2.5 cm), so the transport of the sputtered particles to the substrate is due to a pure

diffusion process. Consequently, the energy of sputtered particles is low enough to avoid damage of the substrate and the growing film.

To solve short channel effects in the downscaling of devices, the planar CMOS transistors are being gradually replaced by three-dimensional architectures that increase the drive current, despite a more complex fabrication route: the FinFETs. Along with dimension reduction, they present higher performance (switching speed) and less power consumption. In this kind of transistors the channel is not flat, but it is folded, forming a Si *fin*. However, these architectures raise reliability questions. This thesis provides a thorough study of the reliability of three gated bulk FinFETs, with a TiN/HfO_2 gate stack and an ultra low equivalent oxide thickness (EOT), in order to ensure that integrated circuits will withstand operation conditions at least for 10 years. Particularly, the mechanisms of the degradation of transistors analyzed in this thesis are the time-dependent dielectric breakdown (TDDB) and the positive bias temperature instabilities (PBTI).

Thin high κ films were characterized by several techniques, such as Fourier transform infrared spectroscopy (FTIR), transmission electron microscopy (TEM), glancing incidence X-ray diffraction (GIXRD) and X-ray photoemission spectroscopy (XPS). Metal-insulator-semiconductor (MIS) capacitors were fabricated by e-beam evaporation of the metal gate and a lithography patterning step for capacitance and conductance measurements.

The Sc_2O_3/Si interface was analyzed by HPS deposition on Si substrates differently prepared: H-terminated Si, native SiO_2, nitrided Si and deposited SiN_x. Nitrided Si and deposited SiN_x present several advantages over native SiO_2 and H-terminated Si: a higher dielectric constant, an oxygen diffusion barrier behavior and a higher quality of the dielectric/Si interface. However, since SiN_x puts a limit in the EOT ultimate scaling, it was decided to use H-terminated Si substrates in the following experiments. A relative permittivity of ~9 was found for the Sc_2O_3 films.

Different deposition conditions were explored for ScO_x thin films to evaluate its properties and its interface with Si. Al/ScO_x/Si MIS devices were fabricated. High deposition pressures (above 1 mbar) reduce interface SiO_x regrowth, increase the quality of the interface and reduce the flatband voltage shift. With this, the advantage of high pressure conditions in reducing the plasma damage to the

substrate was shown. The Al gate reacts with the ScO_x, forming an aluminate that degrades the effective permittivity of the high κ dielectric.

Gd_2O_3 films were deposited on Si with different conditions of pressure. The oxygen solvent Ti and the non-reacting Pt were evaporated for MIS fabrication. While the Pt does not react with the dielectric in the MIS devices, the Ti gate reduces the SiO_x interfacial layer, greatly decreasing the EOT of the stack. As in the case of ScO_x, deposition pressures above 1 mbar shows lower SiO_2 regrowth, lower densities of interface defects, and lower flatband voltage shifts. The Gd_2O_3 films react with the underlying Si and form a silicate during the forming gas anneal at 450 °C. This $GdSiO_x$ decreases the effective permittivity of the dielectric stack and thus increases the EOT. An effective relative permittivity of 11 was calculated.

Amorphous 8 nm thick $Gd_{1.8}Sc_{0.2}O_3$ films were grown by an alternating deposition of Sc_2O_3 and Gd_2O_3 nano-laminates and a post-deposition anneal in forming gas. The ternary oxide shows better thermal stability with Si than its binary components, after two anneals at 300 and 450° C. Additionally, it maintains the amorphous character. $Pt/Gd_{1.8}Sc_{0.2}O_3/Si$ MIS capacitors were electrically characterized, presenting no SiO_x interface, with low density of defects, hysteresis, and leakage currents. A relative permittivity of 25 is found for these devices, which is a great value for the application of this material to the CMOS technology.

Lastly, the reliability of triple gated bulk n-type FinFETs with sub 1 nm EOT was studied through the TDDB and PBTI measurements. TDDB results are analogous for FinFETs and planar devices with 10^{-8} cm^2 area and 0.8 nm EOT, indicating that the breakdown behavior is not affected by the three-dimensional architecture. It is difficult to evaluate TDDB for lower EOTs due to the leakage currents both for FinFETs and planar devices. However, for smaller areas, the extrapolated voltages at 10 years lifetime are 0.7 V, which is below the specifications. Regarding PBTI, gate voltage overdrive (difference between gate voltage and threshold voltage) at 10 years lifetime is lower for thinner EOTs due to the higher reduction of interlayer thickness. Although values are higher than for planar devices, their values do not meet specifications for EOTs below 0.7 nm. Thus, although it can be improved by corner rounding processes, PBTI degradation is going to be a problem in the next generations of Si devices. A higher density of

traps in the top-wall of the fin than in the sidewall was measured, and it degrades PBTI in wider fin devices.

Among future experiments, new processes for the deposition of gadolinium scandate will be designed in order to control its stoichiometry and thickness. The thermal stability and the crystallization temperature of $Gd_{2-x}Sc_xO_3$ as a function of the composition and the growing conditions will be measured. Also, one of the main objectives will be the further reduction of the EOT of $Gd_{2-x}Sc_xO_3$ films by the use of thin Ti films. Besides, e-beam evaporation will be substituted by sputtering deposition of metal gates, with the introduction of materials such as Ta, TaN and TiN. The high κ dielectrics studied in this thesis are currently being deposited on III-V substrates (InP) and SiGe substrates. Other planned research line is the fabrication of metal insulator metal (MIM) capacitors (or resistive switches) with Sc_2O_3, Gd_2O_3 and $Gd_{2-x}Sc_xO_3$ as high permittivity dielectrics for their application in dynamic random access memories (DRAM) cells.

RESUMEN

La tecnología de circuitos integrados CMOS (*complementary metal-oxide semiconductor*) basada en silicio (Si) ha dominado en la industria microelectrónica desde finales de los años 80. Esto ha sido posible gracias a la continua reducción de las dimensiones del principal dispositivo activo: el MISFET (*metal-insulator-semiconductor field effect transistor*). Una de las claves en el escalado de los MISFET fue el dieléctrico usado como aislante entre el metal de puerta (Si poli-cristalino altamente dopado o *poly-Si*) y el canal en el semiconductor (Si): el óxido de silicio (SiO_2). De hecho, estos dispositivos han sido denominados tradicionalmente MOSFET ya que el aislante es un óxido del sustrato de silicio. En 2008, el SiO_2 fue remplazado por un dieléctrico de alta permitividad (dieléctrico de alta κ), un dieléctrico basado en hafnio, para superar problemas críticos en el escalado de los dispositivos de Si. La investigación actual está enfocada hacia nuevas estrategias para las próximas generaciones de transistores MISFET, como nuevos materiales de alta κ o nuevas rutas de fabricación de los dispositivos.

El principal objetivo de esta tesis es estudiar dos estrategias diferentes para continuar el escalado de los MISFET. En primer lugar, se investiga una tercera generación de dieléctricos de puerta: óxido de escandio (Sc_2O_3), óxido de gadolinio (Gd_2O_3) y escandato de gadolinio ($Gd_{2-x}Sc_xO_3$). También se estudian metales de puerta para su integración con estos dieléctricos de alta permitividad: aluminio (Al, que es reactivo), titanio (Ti, que es un disolvente de oxígeno) y platino (Pt, que es un metal noble). En segundo lugar, se caracteriza una nueva arquitectura de dispositivo, el transistor de efecto campo basado en *aleta* de Si (FinFET), que es un transistor tridimensional cuyo canal está doblado en lugar de ser plano.

Esta tesis propone el depósito de Sc_2O_3, Gd_2O_3 y $Gd_{2-x}Sc_xO_3$ mediante pulverización catódica de alta presión (HPS). En este sistema de *sputtering* no convencional, la presión de trabajo es aproximadamente 1 mbar, entre dos y tres órdenes de magnitud más alta que en sistemas de *sputtering* típicos. La alta presión acorta el recorrido libre medio de las partículas del gas de proceso hasta las 50 μm. Los átomos arrancados o reflejados en el blanco se termalizan en una distancia corta (1-3 mm), a través de colisiones con los átomos del gas. La longitud de termalización es mucho más corta que la distancia entre el blanco y el sustrato

(2,5 cm), por lo que el transporte de las partículas arrancadas hacia el sustrato se realiza únicamente mediante un proceso de difusión. Por lo tanto, la energía de las partículas cuando llegan al sustrato es lo suficientemente baja como para evitar el daño a la superficie o a la película creciente.

Para resolver los efectos de canal corto en el escalado de los dispositivos, la tecnología CMOS planar está siendo gradualmente remplazada por arquitecturas tridimensionales que aumentan la corriente de drenador, pese a una ruta de fabricación más compleja: los FinFET. Junto con la reducción del tamaño de los dispositivos, la introducción de esta arquitectura supone unas mayores prestaciones (mayor velocidad de cambio de estado) y un menor consumo de potencia. En este tipo de transistores el canal no es plano, sino que está doblado, formando una *aleta* de Si. Sin embargo, la fiabilidad de estas arquitecturas debe ser convenientemente estudiada. Esta tesis proporciona un estudio muy completo de fiabilidad de transistores FinFET de tres puertas, con un apilamiento de puerta compuesto por TiN y HfO_2 y un espesor de óxido equivalente (EOT, de *equivalent oxide thickness*) ultra bajo, menor que 1 nm, con el objetivo de asegurar que los *chips* soportarán las condiciones de operación al menos por 10 años. En particular, los mecanismos de degradación de los transistores analizados en esta tesis son la ruptura del dieléctrico dependiente del tiempo y las inestabilidades por temperatura y polarización positiva (TDDB y PBTI por sus siglas en inglés).

Las películas delgadas de alta κ se caracterizaron en esta tesis mediante varias técnicas, como son la espectroscopia infrarroja por transformada de Fourier (FTIR), microscopía electrónica de transmisión (TEM), difracción de rayos X por incidencia rasante (GIXRD) y espectroscopia de fotoelectrones emitidos por rayos X (XPS). Se fabricaron capacidades metal-aislante-semiconductor mediante la evaporación por haz de electrones del metal de puerta y un paso de litografía para la medida de la capacidad y de la conductancia de los dieléctricos.

Se analizó la interfaz Sc_2O_3/Si mediante el depósito por HPS sobre sustratos preparados de varias formas: Si terminado en hidrógeno (H), SiO_2 nativo, Si nitrurado y SiN_x depositado. El Si nitrurado y el SiN_x depositado presentan ventajas sobre el SiO_2 nativo y sobre el Si terminado en H: una constante dieléctrica mayor, una barrera a la difusión de oxígeno hacia el sustrato y una mayor calidad en la

interfaz dieléctrico/Si. Sin embargo, como el SiN_x pone un límite al mínimo EOT alcanzable, se decidió utilizar Si terminado en H en los siguientes experimentos. Se encontró una permitividad relativa de 9 aproximadamente para las películas de Sc_2O_3.

Se depositaron películas de ScO_x para evaluar sus propiedades y su interfaz con Si en función de las condiciones de depósito. Se fabricaron dispositivos MIS con estructura de Al/ScO_x/Si. Presiones de depósito mayores que 1 mbar reducen el recrecimiento de SiO_x interfacial, incrementan la calidad de la interfaz dieléctrico/Si y además reducen el desplazamiento del voltaje de bandas planas. De esta manera, se demostró la ventaja que muestran las altas presiones para reducir el daño al sustrato durante el depósito. La puerta de Al reacciona con el ScO_x, formando un aluminato que reduce la permitividad efectiva del dieléctrico.

También se depositaron películas de Gd_2O_3 sobre Si con diferentes condiciones de presión. Para la fabricación de dispositivos MIS, se evaporaron puertas de Ti, que es un disolvente de oxígeno, y Pt, que es un metal noble. Mientas que el Pt no reacciona con el dieléctrico en los MIS, la puerta de Ti reduce la película de SiO_x de la interfaz, disminuyendo el EOT del dispositivo. Igual que en el caso del ScO_x, presiones de depósito mayores que 1 mbar muestran menos recrecimiento de SiO_2, menores densidades de estados en la interfaz y menores desplazamientos del voltaje de bandas planas. Por el contrario, las películas de Gd_2O_3 reaccionan con el Si del sustrato y forman un silicato durante el recocido a 450 °C en atmósfera de *forming gas* (N_2 y H_2). Este $GdSiO_x$ hace disminuir la permitividad efectiva del aislante y por tanto aumenta el EOT. Se calculó una permitividad relativa efectiva de 11 para estos dispositivos.

Mediante el depósito alterno de nano-laminados de Sc_2O_3 y Gd_2O_3 junto con un posterior recocido, se crecieron películas de $Gd_{2-x}Sc_xO_3$ amorfo, rico en gadolinio y de unos 8 nm de espesor. Este óxido ternario muestra una mayor estabilidad térmica con el Si que sus componentes binarios tras dos recocidos en *forming gas* a 300 y 450 °C. Además, mantiene su carácter amorfo. Dispositivos MIS con estructura Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si fueron fabricados y caracterizados eléctricamente. Éstos no presentan ninguna interfaz de SiO_x, con una densidad de defectos relativamente baja y unas bajas histéresis y corriente de fugas. Se midió

una permitividad relativa de 25 para estos dispositivos, que es un valor ideal para la aplicación de este material en la tecnología CMOS.

Por último, se estudió la fiabilidad de transistores FinFET de tres puertas, tipo n y con EOT por debajo de 1 nm mediante las técnicas de TDDB y PBTI. Para los FinFETs y los dispositivos planares de 10^{-8} cm^2 y EOT de 0.8 nm, los resultados de TDDB son muy parecidos, indicando que el comportamiento de la ruptura dieléctrica no se ve afectada por la estructura tridimensional. Para EOTs menores, se hace muy difícil evaluar el TDDB para ambos tipos de dispositivos, debido a altas corrientes de fugas. Áreas más pequeñas se acercarían más a los dispositivos utilizados en los circuitos reales. Sin embargo, los voltajes de operación extrapolados para que los chips vivan 10 años son de 0.7 V, lo que está por debajo de las especificaciones. Con respecto al PBTI, el voltaje de *overdrive* (la diferencia entre el voltaje de operación y el voltaje umbral) para que los transistores vivan 10 años decrece con el EOT debido a los bajos espesores de la interfaz de SiO_x. Aunque los valores son algo más altos para los FinFETs que para los dispositivos planares, los voltajes de overdrive no llegan a las especificaciones para EOTs menores que 0.7 nm. Por tanto, aunque los resultados de PBTI puedan ser mejorados con procesos para redondear las esquinas del FinFET, este tipo de degradación va a ser un problema grave en las próximas generaciones de dispositivos de Si. Por otro lado, se midió una densidad de trampas en la puerta superior del FinFET mayor que en las puertas laterales, lo que lleva a una mayor degradación en los dispositivos en los que la aleta de Si es muy ancha.

Entre los experimentos futuros, se diseñarán nuevos procesos para el depósito de escandato de gadolinio para controlar su estequiometria y su espesor. Se medirá también su estabilidad térmica y la temperatura de cristalización del $Gd_{2-x}Sc_xO_3$ como función de su composición y de sus condiciones de crecimiento. Uno de los objetivos principales será continuar con la reducción del EOT de los dispositivos con este dieléctrico con el empleo de puertas de Ti. Además, la evaporación mediante haz de electrones se sustituirá por el depósito mediante pulverización catódica de los metales de puerta, con la introducción de materiales como Ta, TaN o TiN. Los dieléctricos de alta permitividad estudiados en esta tesis se crecen ahora sobre sustratos III-V (como el InP) y sobre Si tensionado (SiGe).

Otra línea de investigación planeada es la fabricación de capacidades metal-aislante-metal (o interruptores resistivos) con Sc_2O_3, Gd_2O_3 y $Gd_{2-x}Sc_xO_3$ como dieléctricos de alta κ para su aplicación en células de memorias dinámicas de acceso aleatorio (DRAM).

CHAPTER I. INTRODUCTION

The complementary metal-oxide-semiconductor (CMOS) integrated circuit technology based on silicon has dominated the microelectronics industry since the late 80s. This has been possible thanks to the continuous reduction of the dimensions of the main active device: the metal-insulator-semiconductor field-effect transistor (MISFET). The key to the success of this technology was the use of poly-crystalline Si (poly-Si) as metal gate and silicon oxide (SiO_2) as gate dielectric. In fact, this device has been traditionally named MOSFET, since the insulator is the silicon substrate oxide. In 2008, poly-Si and SiO_2 were replaced to overcome critical problems in the downscaling of silicon devices. Current research is focused on new strategies for the next generations of MISFETs, such as new materials or new device fabrication routes.

In this thesis, two different approaches to continue with the downscaling of MISFET are studied. In the first place, we investigated high permittivity (high κ) dielectrics –scandium oxide, gadolinium oxide and gadolinium scandate- and metal gates –aluminum, platinum and titanium- as gate stacks. Secondly, we characterized a new device architecture, the FinFET, which is a three-dimensional transistor whose channel is folded instead of planar. This chapter introduces the basics of these two approaches and justifies the interest of this thesis within the field of microelectronics.

I.1 CMOS DEVICE SCALING

MISFETs consist of a metal-insulator-semiconductor (MIS) capacitor between two *pn* junctions reversely biased, which are called source and drain. The formation of a conduction channel in the semiconductor controls the current between the source and the drain. This simple device, which can switch or amplify signals, is the basis of modern microelectronics. This section describes its evolution and the keys to its expansion.

The beginning of the microelectronic industry can be placed in the late 40s, when W. B. Shockley, J. Bardeen and W. H. Brattain discovered the transistor action at AT&T's Bell labs and developed the bipolar junction transistor [1, 2]. Nine years after the discovery, in 1956, the three of them were awarded with the Nobel Prize

for this work. The second big step took place in 1958: J. S. Kilby in Texas Instruments built the first integrated circuit (IC), i. e. a circuit whose all components were on a single piece of semiconductor, with the aim of diminishing the size of electronic circuits and minimizing their cost [3]. A year later, in Fairchild Semiconductor the group headed by R. Noyce also built independently a similar circuit [4], but using the planar process, which could be used industrially. Both are considered as the fathers of the ICs or *chips*, although only J. Kilby was awarded with the Nobel Prize in 2000 for it (R. Noyce died before, in 1990).

The development of the MISFET meant a breakthrough in microelectronics. Although it was originally conceived by J. E. Lilienfeld in 1928 [5], the MISFET was not fabricated until 1960 by M. M. Atalla and D. Kahng [6, 7, 8]. In 1962, F. P. Heiman and S. R. Hofstein integrated a MISFET in an IC for the first time [9]. They used silicon oxide as gate dielectric, and thus these devices were called MOSFETs. Two years later, MOSFETs reached the commercial market. In the early 70s, they came into common use [10], mainly thanks to two key ideas: the CMOS technology (devised by F. Wanlass in 1963 [11]), which greatly reduced the power consumption; and the planar process (developed by J. Hoerni in 1961 [12], although already present in R. Noyce's ICs), which made MOSFET very easy to integrate.

G. Moore observed in 1965 that the number of bipolar transistors in a chip had been doubling every two years, formulating the so-called *Moore's law* [13, 14]. This exponential trend continued in the following years for the CMOS integrated circuit technology and, in fact, it has reached our days. Moreover, it is kept not only by the size of the MISFET transistors but also by their performance. Nowadays, Moore's law serves as the driving force of the microelectronics industry, following the scaling rules stated by R. H. Dennard in 1974 [15].

I.2 HIGH κ/METAL GATE STACKS

One of the key enablers of the downscaling of the MOSFET was the dielectric used in the isolation between the metal gate and the channel in the semiconductor: the SiO_2. The main reason was the possibility of growing thermal SiO_2 with high quality, a low density of interfacial defects (around 10^{10} eV^{-1} cm^{-2}), high breakdown voltages (15 MV cm^{-1}) [16], and a high band gap (8.8 eV). The only

drawback of this dielectric was a low relative permittivity of 3.9 [17], but this was partially solved by the introduction of a nitrided SiO_2 (SiON) in the 90s.

Dimension reduction led to an enormous scaling of oxide thickness. Figure I.1 shows the actual decrease in the oxide thickness until 2008 for low operating power devices. The data are provided by the International Technology Roadmap for Semiconductors (ITRS) [18], which is the forecast of the semiconductor industry provided by a panel of experts, both from industry and academia. Figure I.1 also demonstrates that the gate leakage current rose due to the tunneling current through the dielectric. High leakage currents have two negative effects: unacceptable levels of power dissipation and operating temperature. Moreover, the temperature threatens the reliability and the performance of the transistors. These problems led the industry to substitute the SiON with a dielectric of higher permittivity [19, 20]. That is the reason why IBM and Intel have used Hf-based dielectrics in their microprocessors since 2008 [21, 22].

Using a high κ dielectric, the MIS capacitance could be scaled with a thicker insulator. The equivalent oxide thickness (EOT) is a figure of merit for MISFET transistors that refers to the SiO_2 thickness that would have the same capacitance

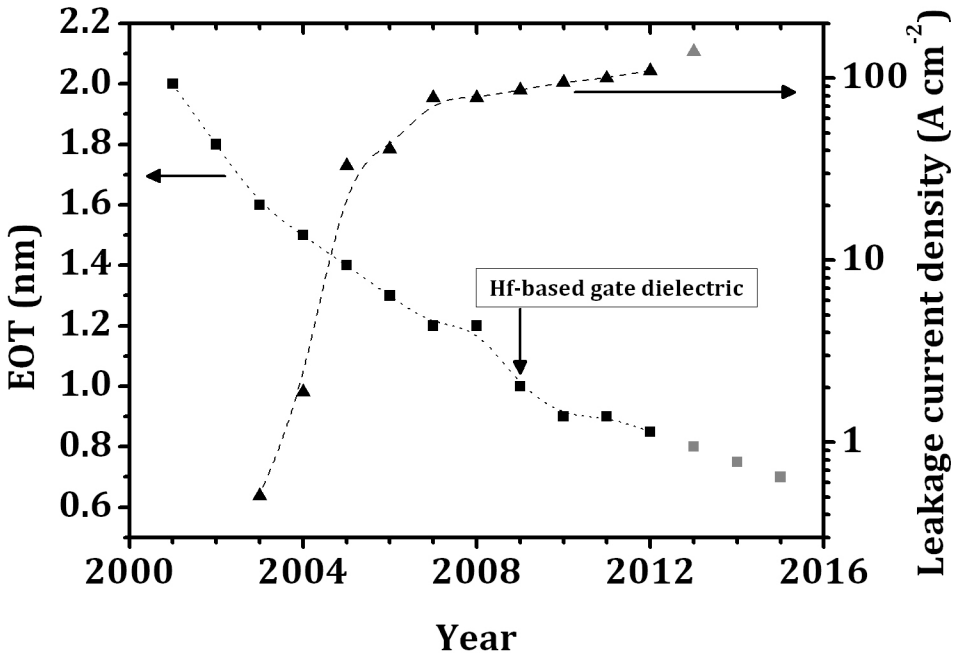

Figure I.1 EOT evolution of the bulk planar MOSFET devices. From ITRS.

as a thicker insulator with higher permittivity. It is defined as:

$$\mathrm{EOT} = \frac{\kappa_{\mathrm{SiO}}}{\kappa_{\mathrm{ins}}} t_{\mathrm{ins}} \qquad \text{equation I.1}$$

where κ_{SiO} is 3.9, the relative permittivity of SiO_2, and κ_{ins} and t_{ins} are the relative permittivity and the thickness of the high κ dielectric, respectively. Figure I.1 shows the evolution of the EOT after the introduction of the Hf-based insulator: the reduction trend has continued but the leakage current density has remained fairly constant.

Highly doped poly-crystalline Si was used as metal gate due to its process compatibility, its stability with the SiO_2 and the possibility of controlling its work function. However, a new effect appeared with the introduction of the high κ dielectrics: the Fermi level pinning [23]. Dipole formation in the poly-Si/dielectric interface modifies the transistor threshold voltages. Thus, the substitution of the poly-Si by a metal became not only optional but also necessary.

A gate stack must fulfill the following requirements to be utilized in an industrial fabrication route [19,24]:

- The relative permittivity value of the high κ dielectric should be above 10 to guarantee scalability in a reasonably number of technology generations, but below 30 to avoid fringe fields from the gate to the source or drain that worsen the short channel effects.
- The conduction band offset from the Si to the dielectric must be above 1 eV to avoid the Schottky emission from the silicon to the high κ material, which contributes to the leakage current. Given that for most materials the conduction band offsets with Si are not symmetrical, this condition implies that the band gap of the insulator must be higher than 5 eV.
- An amorphous dielectric is preferred to a poly-crystalline. The grain boundaries can be a conduction path between the gate and the substrate that increase the leakage current [25]. Moreover, the anisotropy of the crystalline phases can affect the control of the transistor performance.

- The amorphous character must withstand the thermal budget of the process flow.
- The high κ dielectric/Si interface must present a high quality, with a low density of interface defects. These defects trap charge during operation and can decrease the mobility of carriers in the channel by coulomb scattering.
- A low density of bulk defects is needed in the high κ dielectric to avoid charge trapping and leakage paths formation. Trapped charge affects the reliability of the transistor.
- Two different metal gates must be chosen for the p-type and the n-type MISFET, with the work function around the valence band of Si and around the conduction band respectively. Other possibility, worse in terms of performance, is to choose one metal gate with the work function around the mid-gap of Si.
- The Fermi level pinning must be also considered since it can appear in metal/high κ dielectric interfaces.

Figure I.2 depicts the energy band gap and the relative permittivity of the possible candidates for the high κ dielectric [26]. A clear tendency can be observed: higher band gaps imply lower relative permittivities and vice versa. Therefore, this significantly limits the choice of the high permittivity material.

In addition to this, high κ materials are under study in NAND flash memory devices [27]. This kind of devices uses the floating gate MISFET architecture (*flotox*), where a three-layer dielectric -SiO_2/Si_3N_4/SiO_2, called ONO- is sandwiched between a control gate and a floating gate, both of poly-Si. The insulator stack is thus called *inter-poly-Si dielectric*. Due to its great density integration, flotox memories are widely spread in portable devices. According to the ITRS, the inter-poly-Si dielectric will have been replaced by a high κ material by 2017 [18]. Since the device functionality is different, the requirements of the high κ dielectric differ from those of the CMOS technology: they need a very low leakage current to retain charge. Then, a low density of defects and a large band gap with large band offsets are vital. This limits the κ value in the 9-20 range.

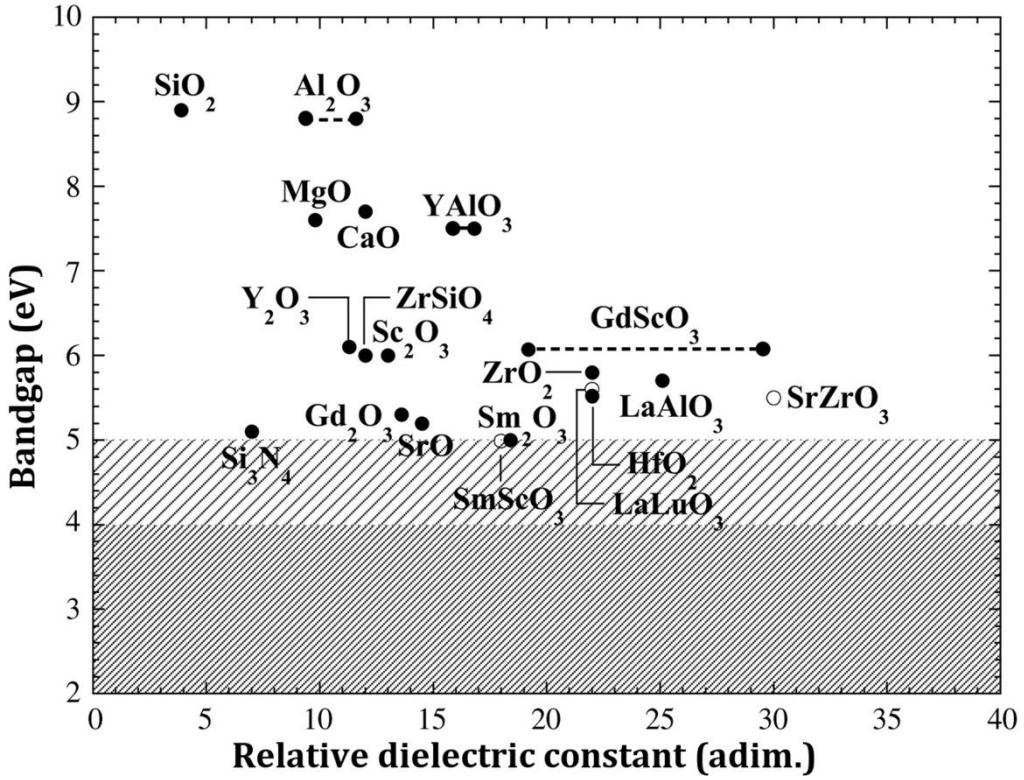

Figure I.2 Relative dielectric constant and bandgap for several high κ dielectrics.

I.3 THE THIRD GENERATION OF HIGH κ DIELECTRICS

The main drawback of the HfO_2 is its low crystallization temperature (around 500 °C) [28]. Currently, it is used in combination with SiON, in order to maintain an amorphous character. Although this HfSiON dielectric presents a higher permittivity than the SiO_2, the κ_{ins} value is not as high as that of the HfO_2, limiting future scalability. For this reason, the pursuit of a third generation of high κ dielectrics becomes necessary.

Ternary rare earth oxides drew interest as possible candidates to replace SiO_2 [26, 29, 30]. Among them, the lanthanum scandate ($LaScO_3$), the dysprosium scandate ($DyScO_3$) and the gadolinium scandate ($GdScO_3$) demonstrated suitable properties for this purpose [31]. Particularly, $GdScO_3$ thin films showed a band gap around 6 eV, a relative permittivity of 22-23, low leakage currents and very good thermal stability in contact with Si (it keeps its amorphous structure with anneals at 1000 °C) [32, 33, 34]. So far, $GdScO_3$ has been grown on Si by pulsed layer deposition (PLD) [31], e-beam evaporation [32], atomic layer deposition (ALD) [33], and metal-organic chemical vapor deposition (MOCVD) [34].

This thesis proposes $Gd_{2-x}Sc_xO_3$ grown by high-pressure sputtering (HPS) in order to substituting the HfSiON-based gate dielectrics. The deposition of this ternary oxide was made by alternating HPS deposition of the binary oxides Sc_2O_3 and Gd_2O_3. Therefore, this thesis begins with the optimization of the growing conditions of these two materials. In fact, Sc_2O_3 and Gd_2O_3 could be candidates by themselves, based on their band gap and relative permittivity [35, 36], as can be seen in figure I.2. Moreover, the three materials (Sc_2O_3 and Gd_2O_3 and $Gd_{2-x}Sc_xO_3$) are also potentially suitable for inter-poly-Si dielectric in flotox memories [27]. Thus, in this thesis, the study of the properties of these materials is focused on their application to both CMOS and flash memory devices.

I.4 HIGH PRESSURE SPUTTERING

A wide variety of deposition techniques have been used for the growth of high permittivity dielectrics [37]:

- Chemical vapor deposition (CVD) based techniques: MOCVD [34], plasma enhanced CVD (PECVD) [38], ALD [33] or photo-assisted CVD [39].
- Physical vapor deposition (PVD) based techniques: e-beam evaporation [32], conventional sputtering [40], plasma oxidation of sputtered metallic films [41], *in situ* thermal oxidation of PVD metallic films [42], solid phase reaction [43] and PLD [31].

CVD based deposition techniques offer complex but flexible depositions. Their main drawback is a high carbon or chlorine contamination from precursors. To avoid it, the film must be grown at a high substrate temperature or annealed at high temperature after deposition. Both solutions lead to the regrowth of a SiO_2 layer in the high κ material/Si interface that reduces the effective permittivity of the dielectric stack. Among the CVD techniques, ALD is seen as the most promising method for the microelectronic industry, since it permits the deposition of conformal films with an accurate control of the thickness, up to the Ångstrom scale. In fact in industrial routes it is the technique of choice for high κ deposition. However, apart from the mentioned contamination problem, a high amount of

precursors are consumed during depositions, which are pollutants, and the chemistry of the reactions is difficult to control.

On the other hand, PVD techniques provide simpler processes, higher purities in the grown films and lower costs. This thesis proposes HPS for the deposition of Sc_2O_3, Gd_2O_3 and $Gd_{2-x}Sc_xO_3$. In the sputtering systems, the structure and physical properties of the films depend on the energy of the particles that reach the substrate. In this nonconventional sputtering, the working pressure is around 1 mbar, between two and three orders of magnitude higher than typical sputtering systems. The high pressure shortens the mean free path of the processing gas up to 500 μm. The sputtered and reflected particles from the target thermalize within a short distance (1-3 mm), through gas collisions. The thermalization length is much shorter than the target-substrate distance (2.5 cm), so the transport of the sputtered particles to the substrate is due to a diffusion process. That is, they reach the substrate with an energy similar to k_BT, where k_B is the Boltzmann constant and T is the temperature. Consequently, the energy of sputtered particles is low enough to avoid damage of the substrate and the growing film.

This technique has been successfully used to grow high-T_c superconductors [44, 45] and our group used it to deposit TiO_2 and HfO_2 high κ dielectric films [46, 47, 48]. It also permits ternary compounds to be grown with a multitarget system which is a very interesting characteristic to pursue scandates research. Simultaneously to this thesis, studies are being performed about oxidation of metallic films, deposited by HPS [41, 42].

I.5 MULTIPLE GATE ARCHITECTURES

The channel length downscaling brings problems for the control of the MISFET performance: the short channel effects [49]. To solve them, the planar CMOS is being gradually replaced by three-dimensional architectures that increase the drive current [50, 51, 52], despite a more complex fabrication route, especially the lithography and patterning steps. Along with dimension reduction, they present higher performance (switching speed) and less power consumption. In this kind of transistors the channel is not flat, but it is folded, forming a *fin*. Two or three sides or even the whole fin can be the channel of the transistor, giving rise to

several types of 3D architectures. They thus present potential area benefits and their name is multigate field effect transistor (MUGFET) or FinFET. Intel announced in May 2011 that triple gated transistor would be introduced in the following generation of microprocessors [53], and they provided a scheme of their FinFET, represented in figure I.3.

Nevertheless these architectures raise reliability questions. This thesis presents a thorough study of the reliability of three gated bulk FinFETs, with a TiN/HfO_2 gate stack and an ultra low EOT. The structure of the FinFETs used in this thesis is described in chapter II. The time-dependent dielectric breakdown (TDDB) and the positive bias temperature instabilities (PBTI) are mechanisms of the degradation of transistors and their assessment methods are described in chapter III. The reliability study must ensure that chips will withstand operation conditions at least for 10 years.

I.6 Outline of the thesis

Chapters II and III constitute a review of all the fabrication and characterization techniques used through this thesis. The HPS, used for high κ deposition, is presented in great detail in chapter II, as it is the core technique of this thesis. Chapter II also describes the fabrication routes of the samples, including the FinFETs devices. Chapter III deals with electrical and physical characterization of the grown films. Among the electrical techniques, this chapter describes the methods used for the reliability study (TDDB and PBTI). It also gives a brief review of the MIS capacitor theory.

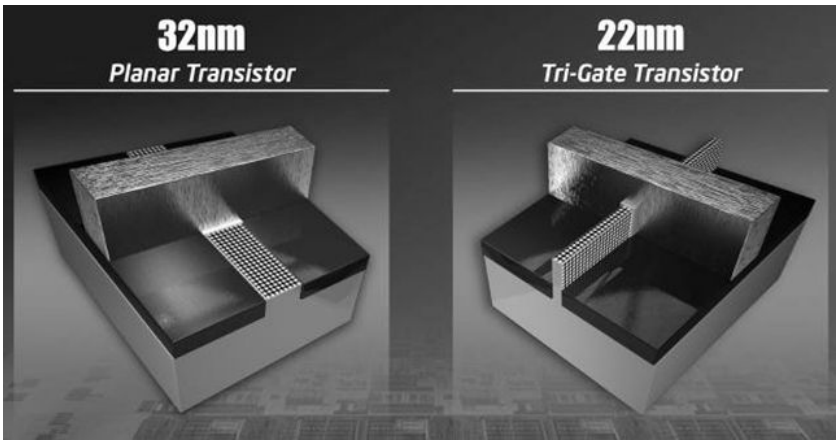

Figure I.3 FinFET architecture. From Intel.

In Chapter IV, the Sc_2O_3/Si interface is analyzed by the comparison of Sc_2O_3 deposition of differently prepared Si substrates. SiO_x and SiN_x are studied to improve the quality of the interface. Although SiN_x supposes an interface with slightly higher quality, it puts a limit on the reduction of the EOT, so the direct deposition on Si is chosen in the following experiments.

Chapters V and VI study the optimization of growing conditions of Sc_2O_3 and Gd_2O_3 respectively. The main conclusion is that higher pressures during deposition lead to interfaces with Si with better quality. These works serve to combine the deposition of both binary oxides to deposit gadolinium scandate films.

Chapter VII presents the results of the $Gd_{2-x}Sc_xO_3$ grown by annealing Sc_2O_3 and Gd_2O_3 nano-laminates. The ternary oxide is compared with its binary compounds. Better thermal stability and an outstanding relative permittivity of 25 are found.

Chapter VIII summarizes the assessment of the reliability of ultra low EOT FinFET, work developed in collaboration with Imec (Leuven, Belgium). TDDB and PBTI are evaluated and the results are compared to planar devices.

Chapter IX finishes this thesis with a brief summary of the work, the most important conclusions, and some guidelines for future experiments.

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CHAPTER II. FABRICATION TECHNIQUES

Microelectronic device manufacturing covers diverse processes such as deposition, etching or lithography. The fabrication techniques used in this thesis are studied through this chapter. Firstly, high pressure sputtering (HPS) is thoroughly described as it is the workhorse in this thesis for high κ dielectric deposition. Its advantages against other deposition techniques are explained. It is followed by the description of the other non-standard deposition technique used, the electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR-PECVD). As it will be seen in chapter IV, this technique was used for the growth of a SiN_x buffer layer between the dielectric and the Si. After that, the metal-insulator-semiconductor (MIS) devices fabrication process is explained. It consists of several steps that include lithography, electron beam evaporation and thermal treatments, which are conveniently discussed. Then, substrates preparation are introduced. The chapter concludes with the description of the fin field effect transistor (FinFET) architecture with ultra-low equivalent oxide thickness (EOT). This kind of transistor constitutes a different approach to continue with the scaling of Si MOSFETs as it was seen in chapter I and the study of its reliability is an important part of this thesis (chapter VIII).

II.1 HIGH PRESSURE SPUTTERING (HPS)

Sputtering is a deposition technique that consists in essence in hitting with plasma ions a target of the material that is meant to be deposited. Atoms are extracted from the target and they travel through the plasma until they reach the substrate, where they are deposited. In HPS, due to the high pressure, sputtered particles thermalize within a short distance in spite of their large initial energy (around 10 eV) [1]. This means that they lose their energy excess in collisions with plasma particles. Thus, they reach the substrate by a pure diffusion process. The aim of this thermalization is to avoid damaging the substrate surface during film growth.

This section is organized as follows: firstly, the experimental system is described (sub-section II.1.1), and then, different theoretical aspects about sputtering are discussed: sub-section II.1.2 deals with plasma collision processes;

sub-section II.1.3 studies plasma shape; and finally, transport and thermalization of the sputtered particles are analyzed in sub-section II.1.4. This section finishes with sub-section II.1.5, where the glow discharge optical spectrometry (GDOS) is described, as a powerful tool to analyze the species that can be found in the plasma.

II.1.1 SYSTEM DESCRIPTION

Figure II.1 shows a simple scheme of the HPS system. This equipment was developed in the *Institut für Festkörperforschung* (IFF) of Jülich (Germany) by the group directed by Dr. U. Poppe for the deposition of superconducting films [2, 3, 4, 5]. Later, it was upgraded for the deposition of high κ dielectrics by the *Láminas Delgadas y Microelectrónica* research group, in the *Universidad Complutense de Madrid* [6, 7].

The system consists of a vacuum chamber where the target, heated substrate holder and generated plasma are located. In order to minimize contamination, the chamber is evacuated until the high vacuum regime is reached before deposition. It typically takes several hours, reaching values between 7×10^{-7} and 1.4×10^{-6} mbar. For deposition, Ar is continuously introduced into the chamber up to pressures in the mbar range. To avoid overcharging the turbomolecular pump, the pumping speed is reduced by using a guillotine valve. Then the plasma is ignited by a radio

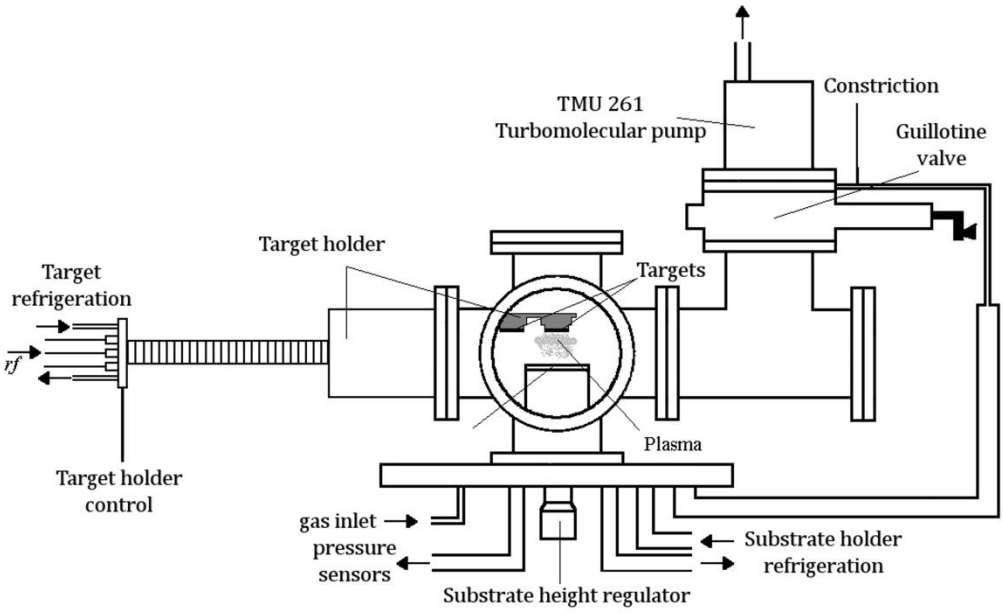


Figure II.1 Schematic of the high-pressure sputtering system.

frequency (*rf)* excitation voltage applied to the target, which acts as one of the electrode of the system. The plasma is composed of electrons, neutral and ionized Ar atoms, and neutral and ionized atoms sputtered from the target. The substrate and the walls of the chamber are grounded and they together serve as the second electrode of the system.

The system is equipped with a mechanical arm that has one axis movement (controlled by computer) and allows the possibility of holding simultaneously three targets of different materials. These targets are glued to the *rf* electrode by a *Varian Torr-Seal* epoxy resin. This resin is specially indicated for vacuum applications due to its low vapor pressure. It withstands pressures as low as 10^{-9} mbar and temperatures from -45 to 120 °C. To avoid resin degradation due to high temperature, the target electrode is refrigerated by a continuous water flow.

Commercial Sc_2O_3 and Gd_2O_3 targets of 99.95% nominal purity, 5 cm-diameter and 3 mm thickness were used through this thesis. They were bought to the company *Goodfellow* and their purity is the maximum provided by the manufacturer.

The three-target-holder mechanical arm is designed so the *rf* signal can be applied to each target separately. Thus each one incorporates its own *rf* connector. The electric discharge is generated by *Hüttinger PFG 300 rf* sources, that have a standard frequency of 13.56 MHz and a maximum output power of 300 W. This frequency is utilized because is one of the frequencies designated by the international communications authorities at which electromagnetic energy can be irradiated without interfering with other radio-transmitted signals.

Sputtering of metallic targets is simpler than sputtering insulators: either alternate current (AC) or a direct current (DC) with standard short-circuit protection can be used. However, insulator targets (as is the case of Sc_2O_3 and Gd_2O_3 used in this thesis) require an AC signal. Otherwise, the target surface would charge fast and the discharge would be interrupted within 1-10 μs [8]. For alternate signals, during the first half cycle (negative voltage), the target is sputtered by positive ions of the plasma while a positive charge is accumulated in the target surface. In the following half cycle (positive voltage), this positive charge is neutralized by electron bombardment. The frequency of the signal must be high

enough to maintain the glow discharge over the full period of the AC waveform. Thus, only *rf* sources can be used. Nevertheless, with the AC signal, charge accumulation on the target surface can also happen. The *rf* source is prepared to measure the DC voltage due to this charge. In all experiments through this thesis, the DC bias was very low: the maximum that was observed was 2 V, and in most cases, it was 0 V.

An *impedance matching network* is required between the source and the target electrode with two purposes. On the one hand, it avoids the reflected power and protects the *rf* generator. On the other hand, it assures that the maximum power from the *rf* generator is coupled to the discharge. It should be connected as close as possible to the target electrode to minimize power loss when the system is not in its matching conditions. In fact, the triaxial cable connecting source and matching network is 5 m long while the one between the network and the system is only 80 cm long. The matching network consists of a set of capacitances and inductances. The values of two capacitances are tunable so the reflected power can be minimized. In all cases through this thesis, reflected power could be completely avoided.

In figure II.2, a schematic of the gas input system is depicted. It is composed of three lines to introduce Ar, N_2 or O_2, although in all plasmas in this thesis only Ar was injected. Each line includes 1/4'' (0.6 cm) diameter steel tubes, a filter, a mass flow controller (MFC), a non-return valve and a manual valve to close the line. The flow of each gas is controlled by a *Bronkhorst Hi-Tec* MFC, with a maximum flow of 40 sccm. An additional low purity Ar line is used to vent the chamber when charging and discharging samples.

The pressure inside the chamber is measured with three sensors, depending on the pressure range. Starting from the highest pressure, from 10 to 10^3 mbar, a *Leybold-Heraeus Kat. Nr. 160 40* is used. The sensor *Leybold TM-20* measures pressures between 10^2 and 10^{-3} mbar, and it is based on a thermal conductivity gauge. Finally, for pressures ranging from 10^{-3} to 10^{-9} mbar, pressure is measured by a *Balzers TPG300*, which is a cold-cathode ionization vacuum gauge.

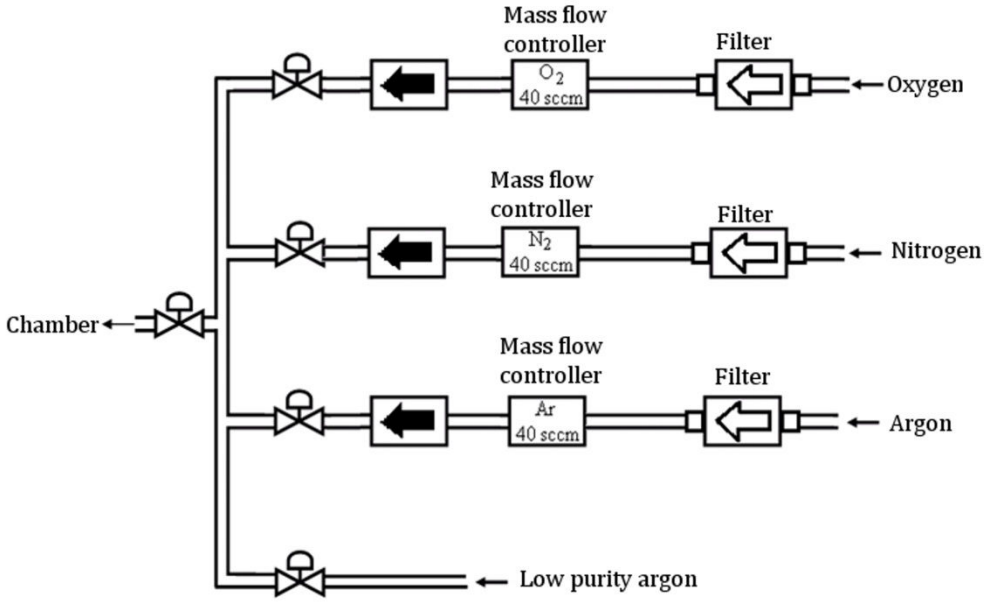


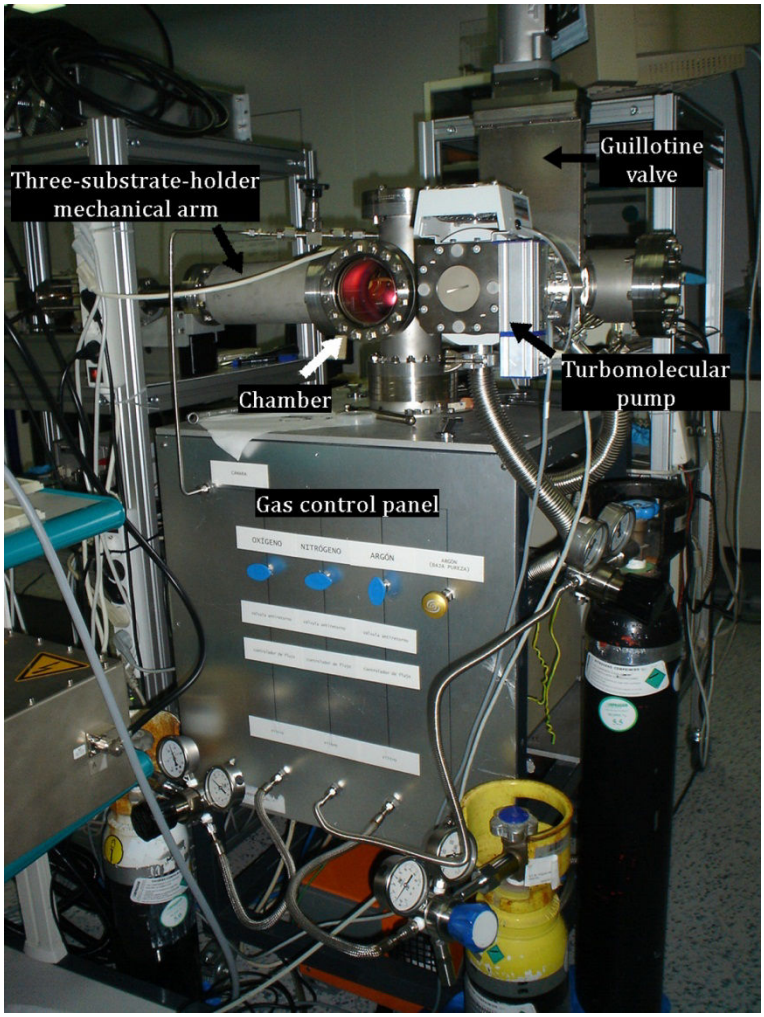
Figure II.2 Gas panel assembly of the HPS system.

The main vacuum pump of the HPS system is a *Pfeiffer TMU 261* turbomolecular pump. It is attached to the chamber through a guillotine valve, which is used to separate the pump system from the chamber when it is opened or to reduce the pump speed. This turbomolecular pump is supported by an *Alcatel Drytel 31* vacuum pump. The ultimate pressure obtained in the HPS system is around 7×10^{-7} mbar.

During processes, the pressure in the chamber is kept constant, ranging from 0.25 to 1.5 mbar. To maximize the process gas flow/leaks ratio, the input flow is the maximum allowable that can be controlled by the MFC (40 sccm) and the pressure is regulated by changing the pumping speed thanks to the guillotine valve.

The substrates are placed on the heated substrate holder that is equipped with a temperature controller. Temperature is measured by a thermocouple and is regulated by a *Eurotherm 818* controller in the range from ambient temperature to 975 °C. The holder allows 2-inch (~5 cm) diameter wafers, and the distance between the target and the substrate can be regulated by means of a micrometer screw. In all experiments, it was fixed at 2.5 cm to keep the substrate away from the plasma region in order to prevent plasma damage to the substrate or the growing film.

(a)



(b)

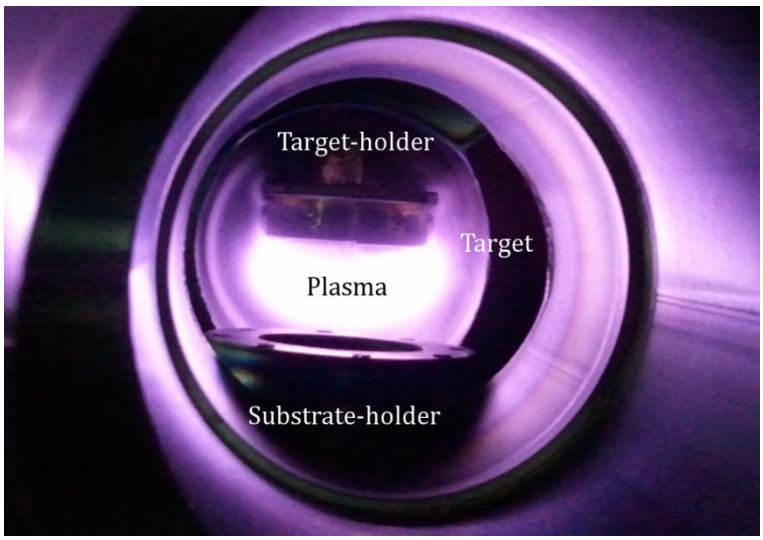


Figure II.3 (a) Photograph of the HPS system. (b) Ar plasma.

A photograph of the HPS system used in this thesis is shown in figure II.3. The next sub-sections describe the processes that happen during sputtering and explain the special characteristics that make this HPS equipment different from other conventional sputtering systems. Sub-section II.1.5 describes the experimental setup that analyses the spectral emission of the plasma during processes.

II.1.2 PLASMAS: COLLISIONAL EVENTS

The basics of the HPS lie in the plasma physics. However, the study of plasmas is an extremely complicated field. In fact, a lot of details of the physics and the chemical interactions between the plasma and the surrounding surfaces are not yet completely understood.

A plasma is a partially ionized gas. It contains as many positive charges (cations) as negative charges (electrons), and also neutral particles (atoms and molecules). The density of neutral particles tends to be much larger than charge density. Many types of processes can happen within the plasma, but the most important are those that include collisions with electrons: ionization, recombination, excitation, relaxation and dissociation. In HPS, the *rf* generator provides the energy required for these processes.

The most important type of collision that sustains the plasma is the ionization caused by an electron impact. In this process, an electron collides with an atom or molecule, and then, another electron is released (figure II.4a). The atom becomes a cation. The two electrons can now produce new ionizations. The opposite process is the recombination, in which an electron reaches an ion and they recombine to form a neutral atom (figure II.4b).

The electron excitation is the movement of an electron to a higher energy state (figure II.4c). The process by which an electron falls from an excited level to a lower energy level is called relaxation and it releases a photon (figure II.4d). This photon has a wavelength that is determined by the difference in energy of the electron states and is characteristic of the atom or the molecule. Thus, the analysis of the emitted spectrum gives very relevant information on the atoms and molecules that are present in the plasma. The acquisition of this spectrum is explained in sub-section II.1.5.

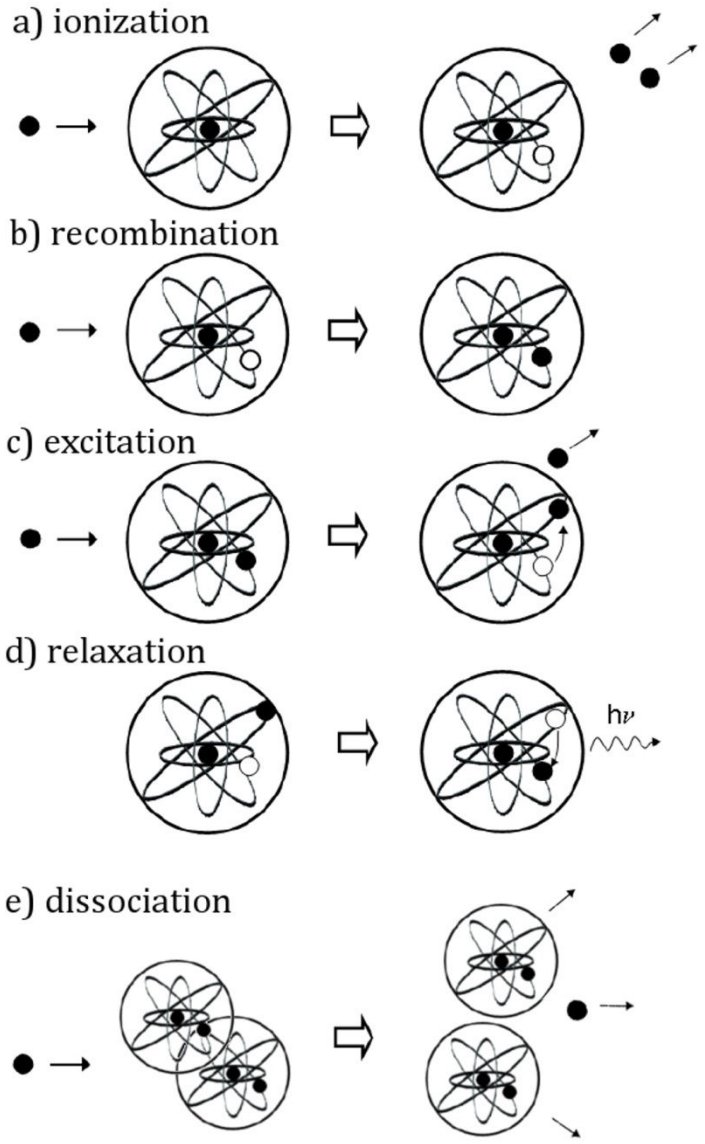


Figure II.4 Collisional events in the plasma involving electrons.

Finally, dissociation can occur when an electron collides with a molecule and separates one or more of its atoms (figure II.4e). In our HPS system this process is very important when the injected gas is N_2 or O_2, since dissociation produce N or O ions that easily react with other species.

II.1.3 VOLTAGE DISTRIBUTION IN RF SYSTEMS

The average speed that the electrons have inside the plasma is very large as compared to the average speed of the ions and neutral particles, since the electron mass is much lower. This also means that the electrons respond almost instantaneously to the alternate electric field, and their positions oscillate within

the cloud of positive charge. Meanwhile, the ions only respond to the time-averaged electric field.

Due to the mass difference, during the first cycles of alternate *rf* voltage the number of electrons that strike the electrodes is larger than the number of positive ions. This happens until an average negative charge is built up in the electrode surface that repels some electrons during the positive halves of the cycles and attracts positive ions more strongly during the negative halves. In the steady state, an equal number of ions and electrons reach the electrode during each complete signal period. This also prompts a negative voltage difference between the electrode and the plasma, which is called sheath voltage, and it is a phenomenon typical of *rf* excited systems known as *self-bias*. These regions around the electrodes are called *dark spaces*, since in this region the charged species are swept away by the field, and thus there is no optical emission.

This effect occurs at both electrodes, so two sheath voltages appear. The ions collide with all surfaces in the chamber, either connected to the *rf* signal or to the ground. However, the geometrical configuration of the electrodes can be adjusted so the sputtering is restricted only to the target surface. Figure II.5 shows a schematic view of the voltage distribution in a *rf* excited discharge. V_1 and V_2 are the sheath voltages of electrodes 1 and 2, respectively, and A_1 and A_2 are their areas. According to the classical treatment of voltage division in an *rf* discharge by Koenig and Maissel [9], the relation between the areas and the sheath voltages at both electrodes follows equation II.1.

$$\frac{V_1}{V_2} = \left(\frac{A_2}{A_1}\right)^4 \qquad \text{equation II.1}$$

From this result, it can be concluded that the larger voltage sheath develops at the electrode having the smaller area. Then, sputtering occurs mainly in this electrode. Connecting the chamber walls and the substrate to ground and the electrode with the target to the *rf* signal makes the area of the grounded electrode much larger than the target electrode area. This way, the target electrode voltage is much higher than the substrate electrode voltage, and it is assured that the sputtering is only appreciable in the target surface while keeping negligible the substrate bombardment.

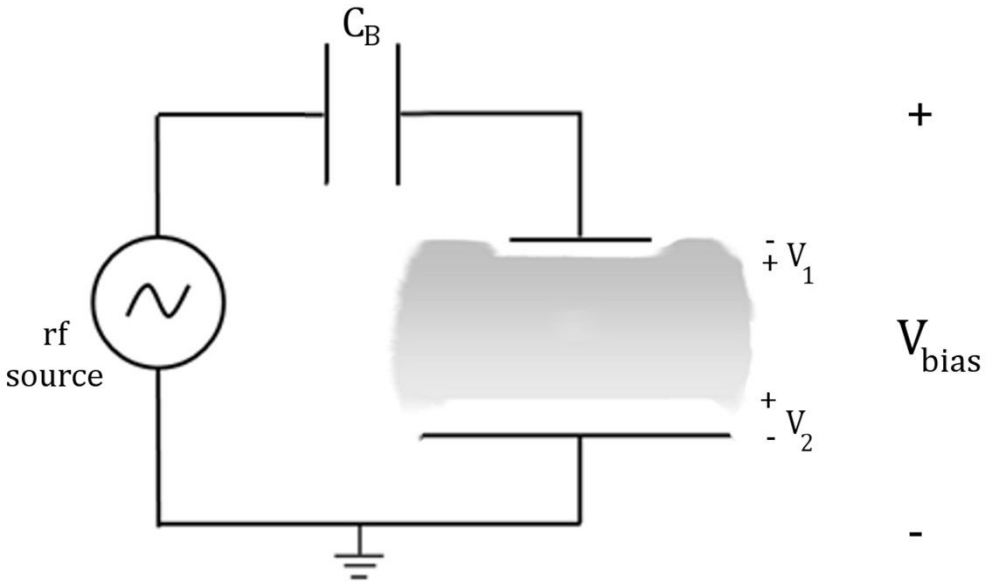


Figure II.5 Schematic voltage distribution in the plasma. C_B is the matching capacitance.

As it was explained above, the ions are accelerated towards the target. Most of these ions end up inside the target, so they become *implanted* particles. A small fraction of the incident ions are reflected with high energy, and they are called *backscattered* particles. As long as the energy of the bombarding ions exceeds the binding energy of the atoms at the surface, the atomic collisions can produce the ejection of particles. The ejected atoms are the so-called *sputtered* particles. Finally, it must be noted that the target also emits secondary electrons.

Secondary electrons are an extra source of electrons to maintain the glow discharge. The sheath voltage leads these electrons towards the glow discharge, providing the plasma with both energy and electrons for the excitation and ionization events. They are called *fast* electrons because of their high energy and they are responsible for a significant transmission of power between the electrodes. They also prompt ionization and excitation in the region close to the target, which is called *negative glow region*. Its high emission is due to the radiative decay of excited and ionized atoms produced by the fast electrons. Figure II.3b shows that this region is confined to the proximity of the cathode.

II.I.4 TRANSPORT AND THERMALIZATION OF SPUTTERED AND BACKSCATTERED PARTICLES

Sputtered and backscattered atoms leave the sheath voltage region around the target and get into the plasma, losing their energy by collisions with the plasma species. Both kinds of particles can reach the substrate with high energy or thermalized (i. e. with energy of the order of $k_B T$). The energy of the incoming species will depend on many parameters, like the chamber pressure, their initial energy and the distance between the target and the substrate. When the energetic species thermalize, they move by a thermal diffusion mechanism, and eventually reach the substrate or the chamber walls, where they produce the growing film. The structure and the physical properties of the thin films grown by HPS depend strongly on the energy of the atoms that reach the substrate. Thus, to get the optimal properties of the film a lot of effort has to be devoted into optimizing the deposition conditions.

The key parameter of the HPS, used to prevent the damage of the interface and the growing film, is the gas pressure. The working pressure in all experiments of this thesis is around 1 mbar, between two and three orders of magnitude larger than conventional sputtering systems. This way, the movement of the sputtered atoms inside the plasma is dominated by diffusion laws. In other words, the sputtered atoms suffer many collisions with the gas environment in a short distance, since the pressure is very high. Thus, they thermalize or lose their energy within a very short distance from the target and they reach the substrate by diffusion.

The thermalization of the sputtered and backscattered particles is due to elastic collisions with the particles of the discharge gas. An analytic model proposed by Valles-Abarca and Gras-Martí [10, 11] estimates the thermalization length in the HPS system. This model takes into account the continuous slowing down of the particles through static gas atoms. The interaction between the particle and a gas atom is assumed to be a screened potential in the form $r^{-1/m}$, where r is the distance between both atoms and m is a coefficient of the interaction ($0 < m < 1$). This calculation also includes the atomic masses and the atomic numbers of the sputtered or backscattered atoms and the gas particles, the plasma

density, which depends on the pressure and the temperature, and the initial energy of the particles.

Table II.1 summarizes the obtained thermalization length values for the sputtered and backscattered particles slowing down in an Ar atmosphere at 1 mbar. The computation is made with the assumption that the sputtered particles are emitted from the target with an energy value close to the surface binding energy (5-10 eV for most solids) while the backscattered particles can reach energies up to 500 eV. Both types of particles interact with the gas atoms through a r^{-4} potential (m = 0.25). As is concluded from table II.1, thermalization lengths are larger for the reflected atoms. However, even those distances are lower than 1 cm, and so they are very small as compared with the distance between the substrate and the target, in the order of 2.5 cm.

It must be noted that the calculations in table II.1 are made with important simplifications. Among them, the most noticeable is considering that the particles move following straight trajectories, neglecting the angular deflections due to the collisions with the static gas atoms. The effect of this error may be appreciable in particles whose atomic masses are close to that of the gas particle. Nonetheless, although the predictions should be only considered qualitatively, this effect would mean that the thermalization length is overestimated. The outcome is that the distance between the target and the substrate is at least an order of magnitude larger than the predicted thermalization lengths. This implies that the particles reach the substrate or the surface of the growing film in a process only determined by diffusion. Thus the damage of the interface Si/high κ oxide and the growing film itself is prevented.

Table II.1 Thermalization lengths in cm for sputtered and backscattered particles in an Ar atmosphere at 1 mbar.

	Sputtered particle			**Reflected particle**
Slowing gas	O	Sc	Gd	Ar
Ar	0.04 cm	0.05 cm	0.05 cm	0.30 cm

II.1.5 GLOW DISCHARGE OPTICAL SPECTROSCOPY (GDOS)

As it was stated above, the plasma of the HPS emits electromagnetic radiation. The spectral analysis of this light emitted by the glow discharge is crucial for explaining the properties of the growing films since it allows the identification of atoms present in the plasma. The HPS is provided with the experimental setup necessary to measure the light spectrum and it is described in depth in this sub-section.

It must be remembered that in a relaxation process the emitted photons have an energy that is the difference between the upper and the lower electron energy level, as was explained in sub-section II.1.2. In the case of atoms and ions, emission spectra are composed by lines of a characteristic wavelength. However, molecules spectra present groups of different intensity around a certain wavelength, which are called bands. This is caused by the fact that the electron energy states in a molecule have a contribution from the vibrational and rotational energy levels of the atom nuclei that form the molecule. The relative intensity of the peaks or bands is proportional to the amount of electrons that are in the upper level and to the probability of the electron transition. This probability is related to the resonance between the electron wavefunctions of the two quantum mechanical states.

A schematic of the experimental system is represented in figure II.6. The light emitted by the plasma reaches a monocromator through a sapphire window, which absorbs only photons with wavelength under 170 nm (energies above 7.3 eV). Since the spectra were recorded from 280 nm up to 550 nm, the window does not affect the measured spectrum. The monocromator *Jobin Yvon H-25* has a resolution of 0.1 nm and consists of an input slot, a system of collimator lenses and a diffraction grating. The diffraction grating selects a certain wavelength from the whole spectrum. The photons with this wavelength move to the photomultiplier where each one stimulates an electric signal. When the photon reaches the photomultiplier, they strike on the photocathode, which emits one electron. An electric field leads this electron to a dynode, which is made of a material prone to emitting secondary electrons, thus emitting two electrons that move to another dynode. After a series of dynodes, a packet of electrons produced by one photon arrives at the anode of the photomultiplier. Therefore, a pulsed signal is obtained,

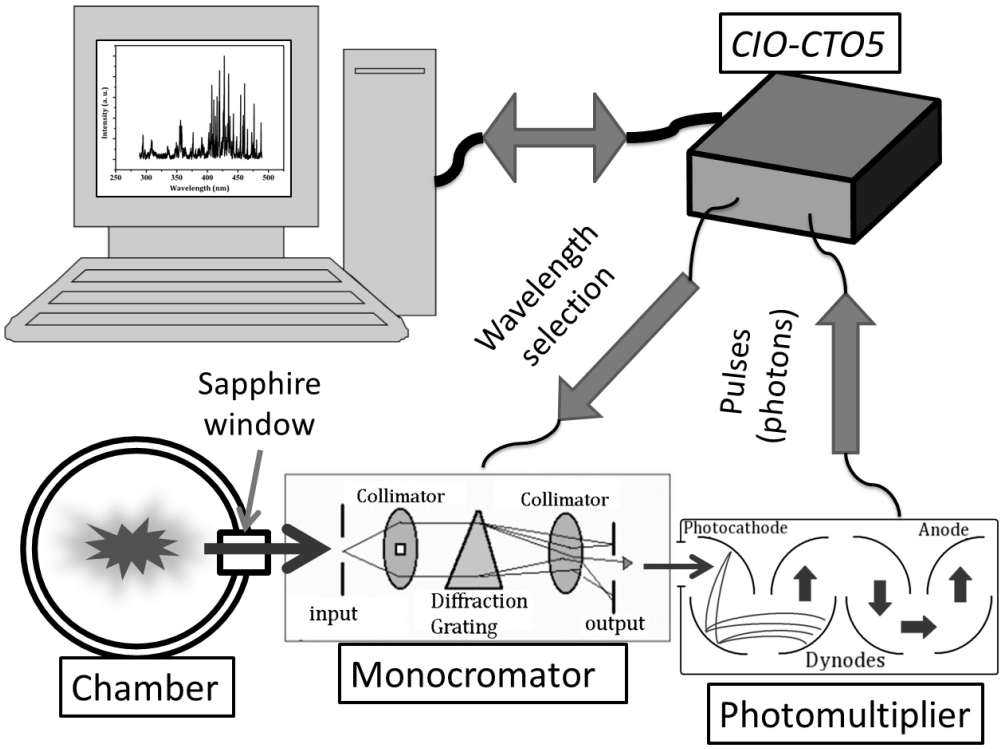


Figure II.6 Glow discharge optical spectroscopy diagram.

where each pulse represents a photon. A *CIO-CTO5* card processes this signal and controls the selection of the wavelength through the diffraction grating. A *LabView* interface communicates with the card, i. e. it allows the user to select the wavelength sweep and to obtain the spectrum.

Through this thesis, plasmas using Sc_2O_3 and Gd_2O_3 targets were analyzed. This technique confirmed the presence of Sc and Gd atoms in the plasma. The relative intensity of the neutral Sc and Gd (called Sc I and Gd I in spectroscopy) peaks as compared to the neutral Ar (Ar I) and the once ionized Ar (Ar II) helps to determine the optimal conditions for the high κ growth.

II.2 Electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR-PECVD)

This system was used for optimization of the interface between the high κ and the silicon, as will be discussed in chapter IV. In this section a brief explanation of the operation of this technique is given. A detailed description can be found elsewhere [2, 3, 4].

Chemical vapor deposition (CVD) is a chemical process often used in the semiconductor industry to grow films [8]. In a typical CVD process, the substrate is exposed to volatile precursors that react on the substrate surface to produce the desired deposit. Plasma enhanced CVD (PECVD) enables the chemical reaction to take place at lower temperatures by helping to activate the precursors with a glow discharge instead of thermal energy only.

When the plasma is produced by an electron cyclotron resonance (ECR) source the technique is known as ECR-PECVD. In the ECR sources the energetic electrons are generated by applying an *rf* electric field with the same frequency than that of an electron in the presence of a static magnetic field. When both frequencies are coupled, the power that the electrons absorb is maximum. In this configuration, the trajectory that the electrons travel along the cyclotron motion is longer. As a consequence, the ECR configuration enhances the chance of electrons to collide with the atoms or molecules of the precursor gases, increasing the activation rate of the species. Therefore, the ECR-PECVD provides a very high activation efficiency. Its main advantage is the possibility of working at lower pressures than PECVD systems, which consequently reduces the gas flow into the chamber.

Figure II.7 shows a simplified scheme of the experimental set, which consists of the following parts:

- plasma source;
- chamber;
- substrate holder;
- vacuum system;
- gas control system.

A commercial *Astex AX4500* reactor is used to generate the plasma. It consists of a quartz chamber where the gas is introduced from one side. The electric field is obtained by an *Astex S-250* microwave source, which gives a 2.45 GHz signal with power up to 250 W. The microwave source is connected to the reactor through a coaxial cable and a slotted waveguide, which has two adjustable stubs to minimize the reflected power. The static and divergent magnetic field is created by an electromagnet which controls the magnitude of the field through the dc current.

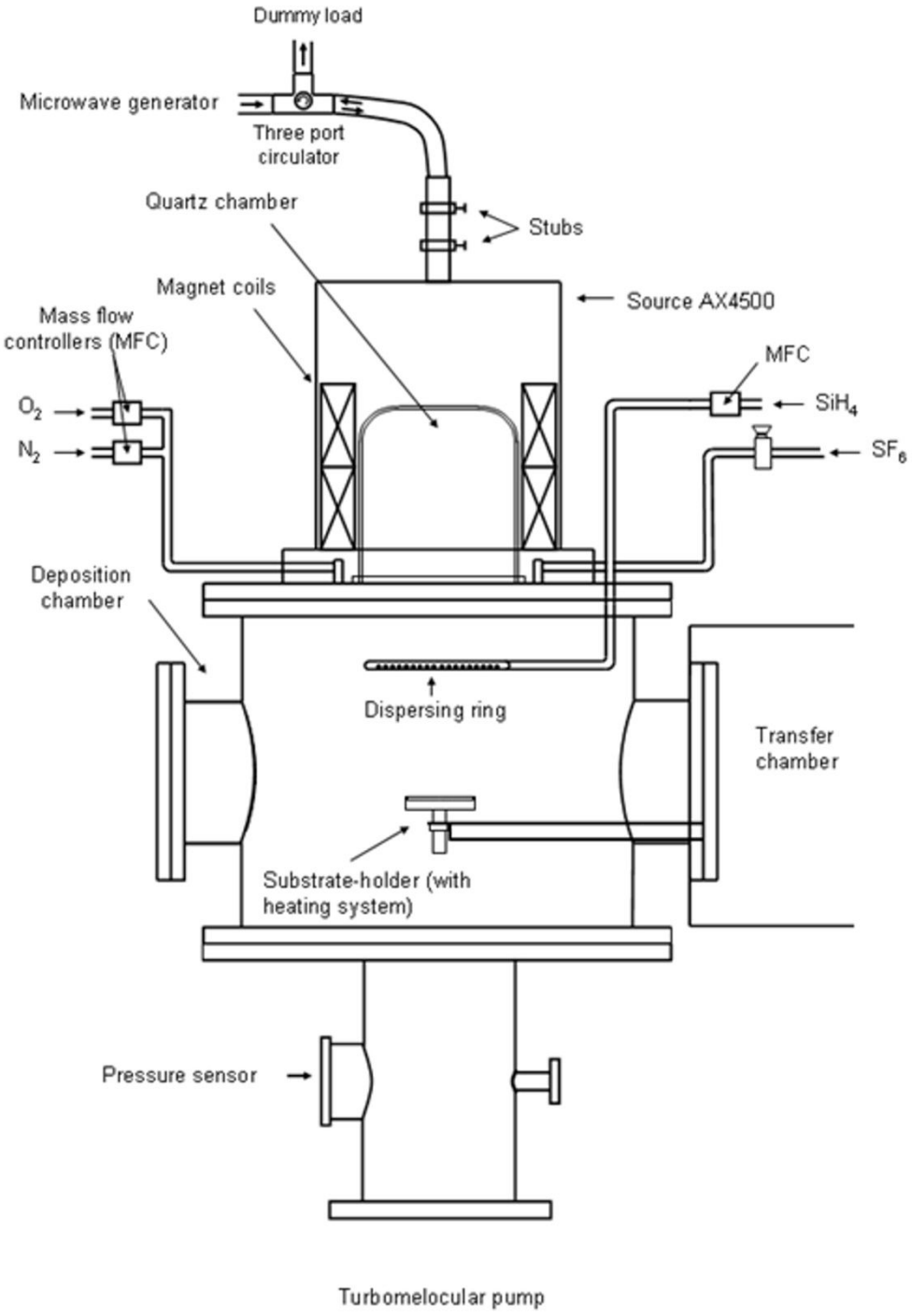


Figure II.7 Diagram of the electron cyclotron resonance plasma enhanced chemical vapor deposition.

The main chamber, made of stainless steel, was also designed by the *Láminas Delgadas y Microelectrónica* research group [12]. The plasma source is located in the upper part of the chamber. The aperture of the chamber is provided with a cover attached to an arm. This arm is the substrate holder. The chamber is opened to a transfer chamber made of acrylic glass. This transfer chamber permits the

cleaning of the substrate in a controlled inert environment, which prevents the silicon surface oxidation. It also avoids chamber contamination, reducing the pumping time by several hours. In the lower part of the main chamber, a turbomolecular pump *TPH 330* is placed, supported by a two-step rotary vane *Duo 030A* pump, both from *Balzers*.

The substrate holder is provided with a heating system and a temperature sensor. The heating is produced by a coiled *Thermocoax* wire. The temperature is measured in the center of the substrate holder by a platinum resistance. The cables for the temperature measurement and the wire supply power are introduced in the chamber by ceramic wall bypasses.

Before each process, the camber reaches vacuum values of around 4×10^{-7} mbar. The process is carried out with pressures in the order of 10^{-3} mbar, three orders of magnitude larger than base pressure. Thus, any kind of contamination can be neglected.

Precursor gases in this thesis were N_2 (5.5 purity) and SiH_4 (3.7 purity). To control automatically the flux of these gases during processes, the ECR-PECVD has a gas control panel similar to that of the HPS (figure II.2). The MFCs of the gases allow a maximum mass flow of 40 and 20 mln min^{-1} for N_2 and SiH_4 respectively.

This system was used in two operation modes throughout this thesis. On one hand, pure N_2 plasma was used for the nitridation of the Si surface. On the other hand, a SiH_4/N_2 plasma was produced in order to deposit a ~1 nm thick SiN_x layer on the Si. The aim of both operation modes was to grow a nitrided Si film on the substrate surface. Silicon nitride is currently used for the passivation of silicon devices because it acts as an excellent barrier against the diffusion of water, sodium and boron. It is also used as a mask for the selective oxidation of silicon. It has the advantage of a slow oxidation and thus it prevents the underlying silicon from SiO_x regrowth. This was used in chapter IV to prevent the oxidation of the Si substrate during the HPS deposit, improving the quality of the high κ/Si interface.

II.3 METAL-INSULATOR-SEMICONDUCTOR FABRICATION

Metal-insulator-semiconductor (MIS) devices were fabricated in order to characterize electrically the high κ films. In the following the fabrication process will be described. In all experiments, a metal was deposited on the high κ insulator by electron beam evaporation. This technique is introduced in sub-section II.3.1. Then, a standard lithography process determined squares of different sizes by means of a lift-off or an etching procedure. Each metallic square defines the top electrode of one MIS device. The lithography steps that were used to define the electrodes are described in sub-section II.3.2. The semiconductor contact was made by the evaporation of a metal (typically Al) on the backside of the substrate wafer. After backside electrode deposition, samples were annealed in a forming gas (N_2 and H_2) atmosphere. The details of this process are explained in sub-section II.3.3.

II.3.1 ELECTRON BEAM EVAPORATION

An electron beam evaporation system was used for the deposition of both electrodes. Figure II.8 shows a scheme of the experimental setup employed along this thesis.

In an electron beam system, a high intensity beam of electrons is focused on a source crucible that contains the material to be evaporated. Electrons are emitted thermionically by a wolfram filament which is placed at a very high potential (~6 kV). A magnetic field created by a magnet deflects the energetic electrons towards the target material. This way, the material is heated and eventually melts. The liquefied material then evaporates to the vacuum due to the vapor pressure. The metal atoms must reach the sample surface without neither colliding nor scattering. Therefore the mean free path of the atoms must be much larger than the dimension of the chamber. For the dimensions of the evaporation system (~50 cm), the working pressure must be at least in the order of 10^{-6}-10^{-7} mbar to achieve this requirement. This way, the atoms reach the substrate following a straight trajectory; they are deposited onto the sample and produce the metallic film. The reduced pressure is reached by means of a turbomolecular pump model *Balzers TPH 330* with the backing of a rotational pump *Balzers Duo 030A*.

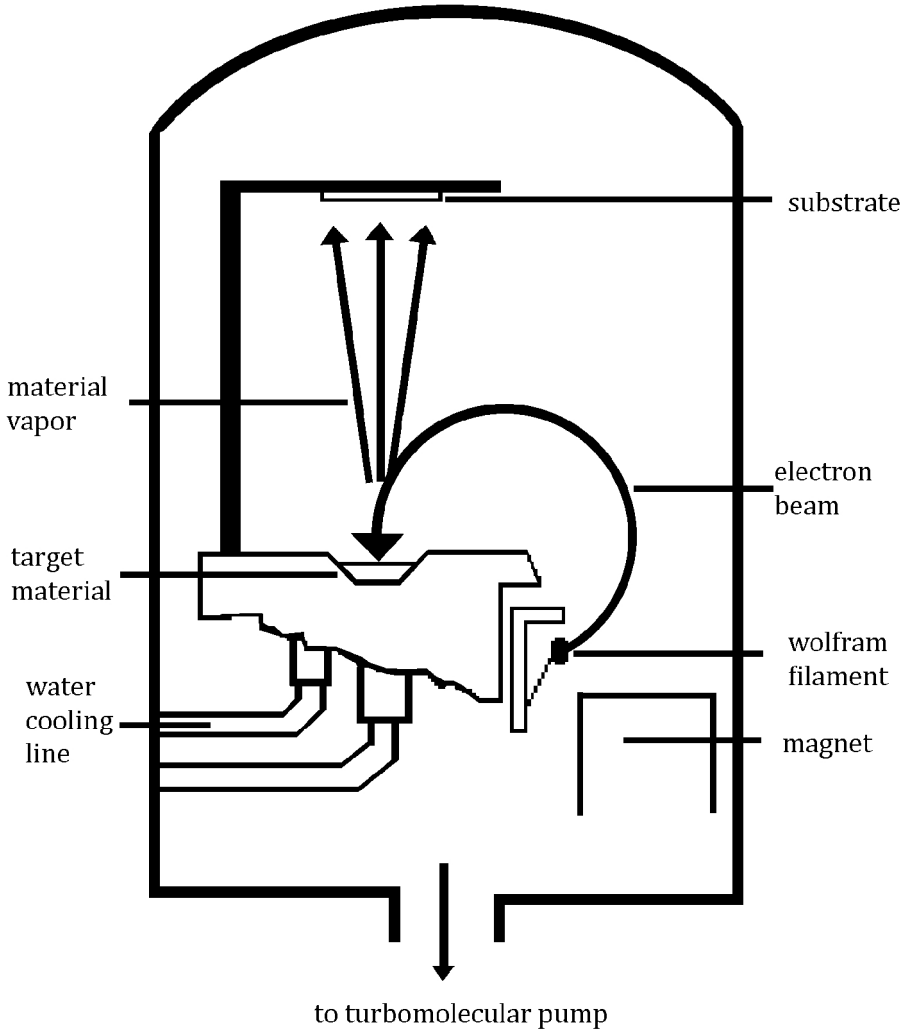


Figure II.8 Electron beam evaporation scheme.

The deposition rate can be controlled by changing the current of the electron beam and/or the energy of the electrons. The deposition rate is monitored by a quartz crystal. The shift of the resonant frequency of the crystal is proportional to the thickness of the deposited films. The deposition rate can be measured with an accuracy better than 0.1 nm s^{-1}.

Several metal stacks for top contact were used for comparison: aluminum (with a thickness of ~300 nm), platinum (with a thickness of ~16 nm to avoid adhesion problems) and titanium (~100 nm thick). Pt and Ti were then capped with a ~200 nm thick Al layer in order to avoid structural degradation during probing and, for Ti, also to avoid surface oxidation. After deposition, the layers

were lifted-off to define the square contacts, with sizes from 50×50 to 630×630 μm^2.

Previously, Al was commonly used as a top electrode. However, it was observed that it is prone to react with high κ dielectrics and form aluminates, thus reducing the effective dielectric constant of the stack. Pt was used to measure the plain properties of the dielectric stacks, since it is a noble metal and does not react with the underlying films. Ti electrodes were also studied because it is known to work as a scavenger of interfacial SiO_x, thus increasing the effective permittivity [13, 14]. The analysis of the effect of the metal gate in the performance of the MIS devices was a very important aspect of this thesis and will be further studied in chapter V.

The bulk contact of the MIS device was fabricated covering the entire back surface of the substrate with a 300 nm thick aluminum layer or a 100 nm Ti/ 200 nm Al stack.

II.3.2 LITHOGRAPHY

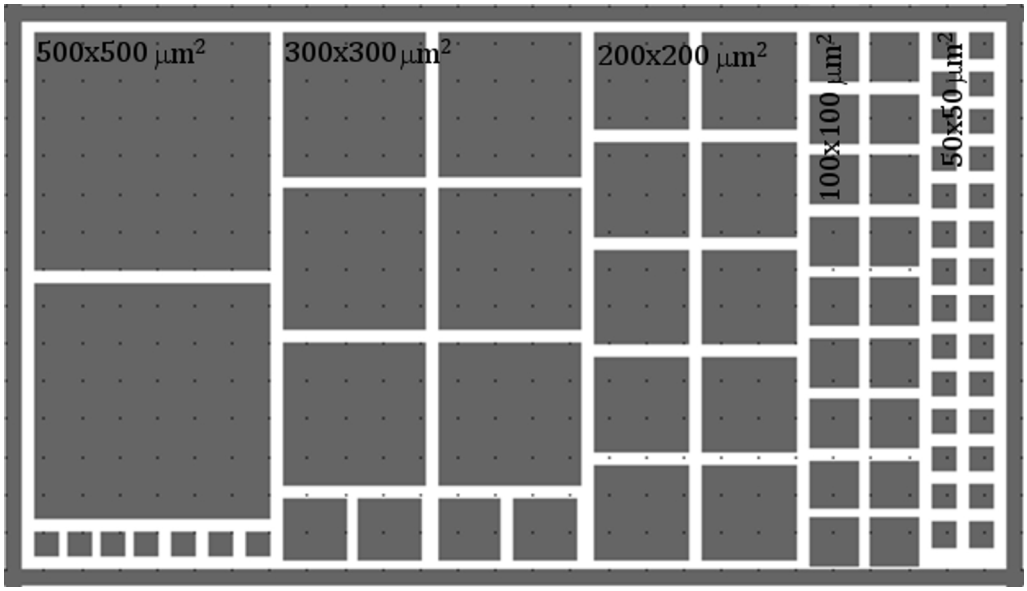
Lithography was used to define the metal top contacts. This process was continuously modified during the thesis in order to improve the results. In this sub-section, three different methods of lithography used in the MIS fabrication will be explained.

At first, the dielectric stack was deposited by HPS on bare Si substrates, followed by top electrode Al deposition. Then a positive photoresist (*AZ® S1838* of *MicroChemicals*) was used for coating the insulator. Afterwards, it was exposed through a mask that defined squares with sizes between 50×50 to 630×630 μm^2. The mask (lithography mask 1) consisted of a repetition of the die shown in figure II.9a. After resist development, the metal layer was etched by submerging the sample in an Al etchant solution (H_3PO_4:HNO_3:CH_3COOH:H_2O). Photoresist was then removed with acetone. This process line was utilized for the experiments of chapter IV.

However, other metal electrodes apart from Al required thorough study but their wet etch was not as simple. Thus, a lift-off process was optimized in order to deposit Ti and Pt as the MIS gate. In this case, a negative photoresist (*AZ® nLOF*

2035 of *MicroChemicals*) was spun on the dielectric layer for coating. The mask used was the same as in the previous route (lithography mask 1 shown in figure II.9a). After exposure and development, the metal stack (100 nm Ti/200 nm Al or 16 nm Pt/200 nm Al) was e-beam evaporated on the photoresist. Then, the metal was lifted off by introducing the sample in the remover NMP (N-Methyl-2-pyrrolidone). This process was carried out for the fabrication of the devices in chapters V and VI.

(a)



(b) (c)

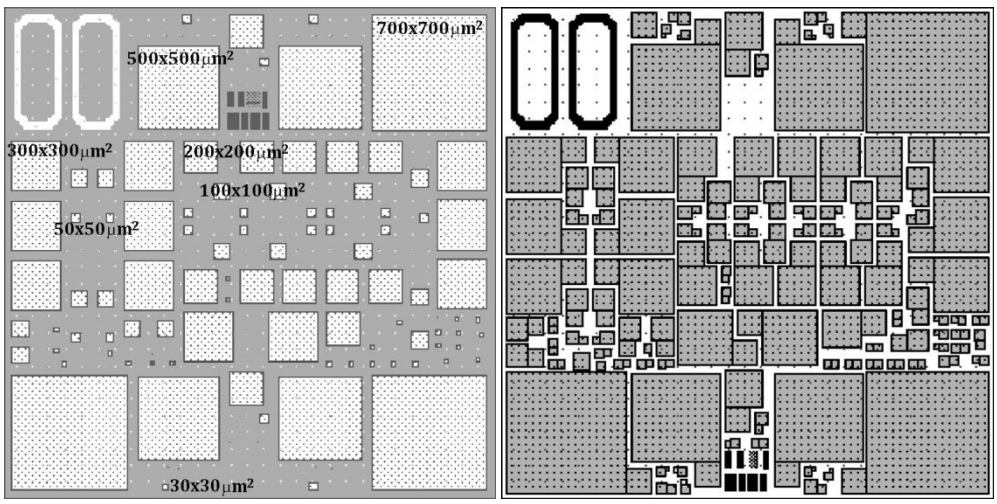


Figure II.9 (a) Lithography mask 1 used for MIS device definition. (b) Lithography mask 2 used for opening windows in SiO_2. (c) Lithography mask 3 used for electrode definition by metal lift-off.

These two process lines defined metal squares on the dielectric, which are directly contacted by a measuring needle in a probe station. Although these approaches are simple from a fabrication point of view, they present a significant hazard. Depending on the pressure posed on the needle and the metal density and thickness, the dielectric film can be locally damaged. This can affect the electrical measurements, specially the leakage current. Then, in order to prevent this problem, a process line was developed, which is explained in the following paragraphs.

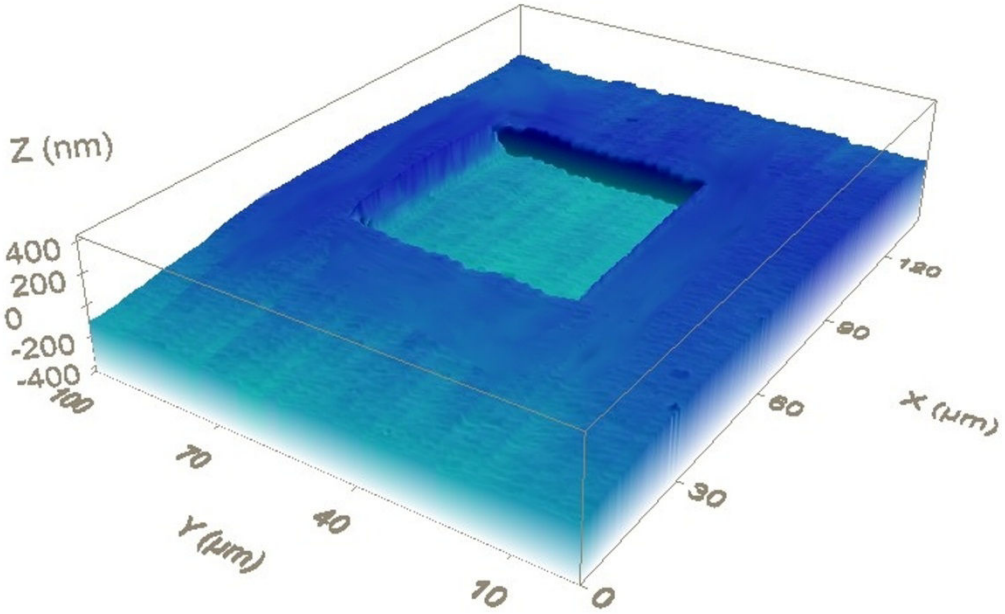
The aim of this fabrication line was to build up pads on thick SiO_2 layers connected to the devices under test. Thus, the first step was to open windows on a thermally grown 200 nm thick SiO_2 layer. The configuration of the windows in a die can be observed in the lithography mask 2 that is represented in figure II.9b. After that, the dielectric stack was deposited. Finally, the metal electrodes were defined by a lift-off process, using the lithography mask 3, shown in figure II.9c. The metal coats the opened windows, which define the MIS devices to test, and a small area of SiO_2 connected to them: the pads. This way, the measuring needle applies pressure only to the pad, located on the thick silicon oxide, instead applying pressure to the thin high κ film. Using a thick SiO_2 layer assures that both the pad parasitic capacitance and the pad leakage current are negligible and thus the electrical measurements of the MIS device are not distorted.

Figure II.10a depicts a confocal microscopy image of a 30×30 μm^2 window opened in the 200 nm thick SiO_2. Figure II.10b shows an image of the device after the metal deposition. It can be observed the device in the window and the pad on the SiO_2.

In this process line the silicon wafers followed the next process steps:

1. Firstly, they were thermally oxidized in a wet atmosphere at 1000 °C during 1 h. This produced a 200 nm thick SiO_2 layer on both sides.
2. Using a positive photoresist (*AZ® S1828*) and the lithography mask 2 of figure II.9b, the square windows with sizes from 10×10 to 700×700 μm^2 were opened submerging the samples in a buffered HF solution for 3 min.

(a)



(b)

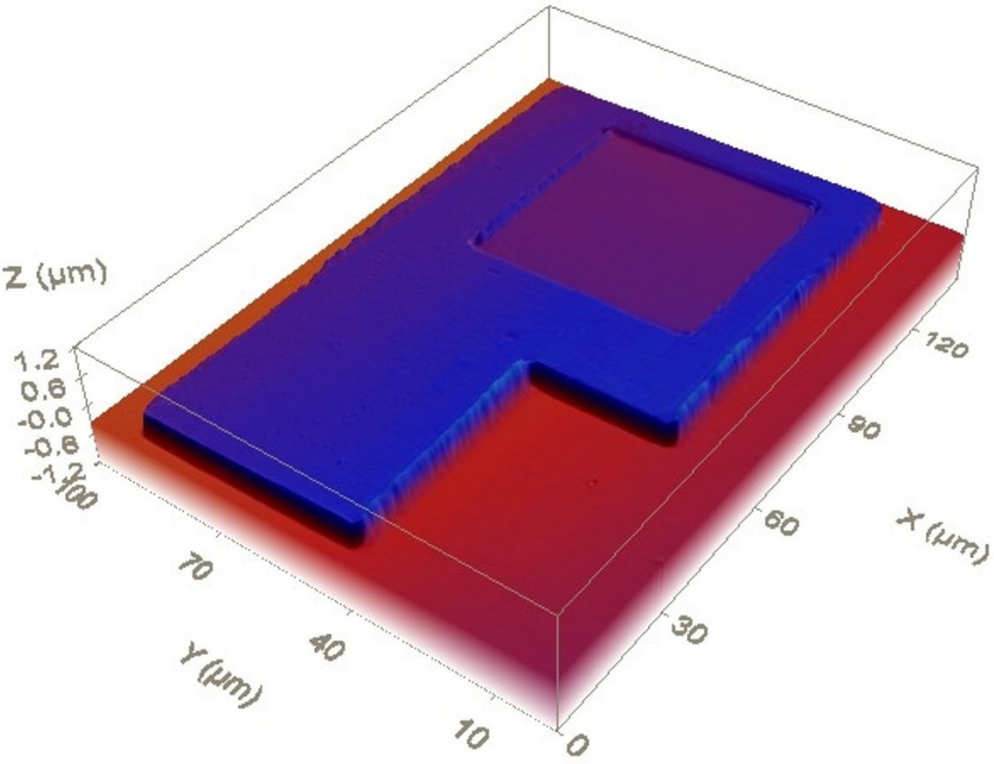


Figure II.10 Steps for metal-insulator-semiconductor fabrication. (a) Window opening of 50×50 µm in a SiO_2 200nm layer. (b) Electrode deposition (definition by lift-off).

3. Then, the Si surface was cleaned by means of a standard RCA clean, which will be explained in next section.
4. The wafers were submerged in a 1:50 HF solution to remove the native SiO_2 immediately before the introduction to the HPS chamber for the dielectric deposition.
5. After high κ deposition, a negative photoresist (*AZ® nLOF 2035*) was used to coat the wafer. Then, it was exposed through lithography mask 3 (figure II.9c) and revealed.
6. Finally, metal was deposited by e-beam evaporation and lifted off with the remover NMP.

This last fabrication line was used with thin high κ ternary compounds ($GdScO_3$) in chapter VII. It is remarkable that this route is much more complicated than previous approaches, but on the other hand, the measured leakages are orders of magnitude smaller than the ones measured on devices fabricated by the simpler routes.

II.3.3 THERMAL TREATMENTS

After MIS fabrication, the samples were annealed in a forming gas atmosphere (90% N_2 and 10% H_2). The annealing consisted in raising the temperature of the sample with a controlled rate and atmosphere, keeping the temperature for a fixed time, and then allowing it to cool. The temperature curve can be observed in figure II.11. Annealing temperatures ranged from 300 to 450 °C and the annealing time was 20 min. This process has two purposes: in the first place, hydrogen atoms can passivate the dangling bonds in the Si/high κ interface, reducing the density of interfacial defects; secondly, it assures the silicon ohmic contact on the backside, reducing the series resistance. It will be seen that the forming gas annealing also catalyzes reactions of the components of the stacks. Thus, formation of silicates or aluminates is observed after the annealing. Ti gates also dissolve the oxygen present in the SiO_x interface during the anneling (scavenging). Through this thesis, the effect of this anneal in the gate stack will be analyzed.

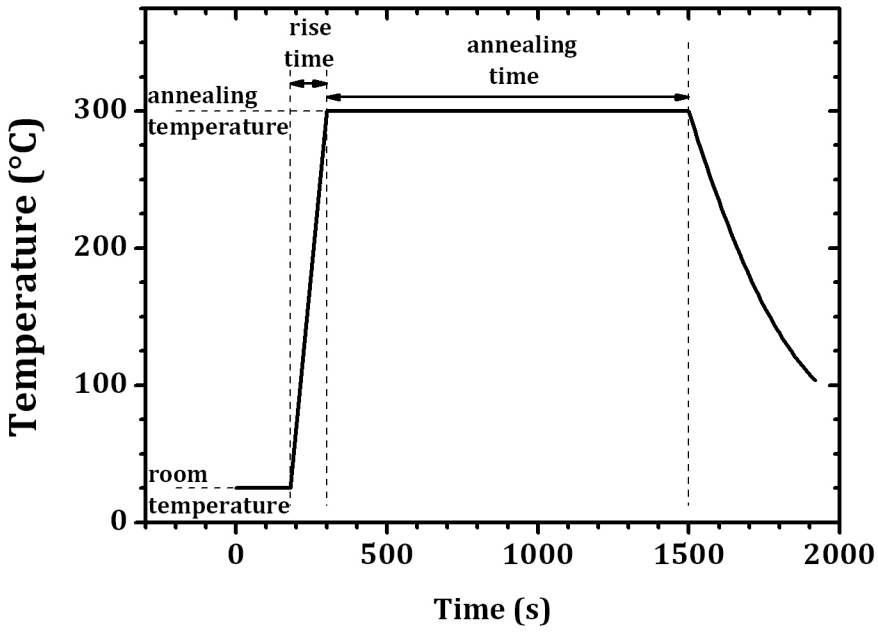


Figure II.11 Temperature curve in the annealing process.

II.4 SUBSTRATES AND SUBSTRATE CLEANING

The high κ stacks were deposited by HPS on 2-inch diameter Si wafers. Depending on the characterization technique, two kinds of wafers were selected. In chapter III, the reasons for these choices will be further discussed.

For Fourier transform infrared spectroscopy (FTIR), floating zone double side polished n-Si wafers with (100) surface orientation and high resistivity (800-1200 Ω cm) were employed. The wafer thickness was 200 or 300 μm. The number of phosphorous dopants was very low in order to minimize the photon absorption by the free charge carriers. These samples were also used for measuring the physical properties of the grown films by ellipsometry, x-ray photoemission spectroscopy, x-ray diffraction…

For MIS fabrication, floating zone low resistivity n-Si wafers were used in order to reduce the series resistance influence on the electrical measurements. One side of the wafer was polished and the surface orientation was (100). The resistivity was 1.5-5.0 Ω cm and it was doped with phosphorus. These wafers were 500 μm thick.

The electronic properties of the dielectric/silicon interface are strongly affected by the chemical integrity and morphological structure of the silicon surface before dielectric deposition [15]. Then, the cleaning procedure is crucial for obtaining high quality interfaces since it removes particles and contamination from the silicon surface.

Through this thesis, wafers used as MIS substrates were cleaned by a procedure called standard RCA clean. This procedure was named RCA after *Radio Corporation of America*, the American electronics company that developed it. It was published by Kern in 1970 although it had been used at RCA since 1965 [16].

The original RCA clean sequence follows this sequence of steps [17]:

- Standard clean 1 (SC1): immersion of the wafer in a solution H_2O:H_2O_2 30%:NH_4OH 29% (5:1:1) at 70-80 °C for 10 min. This clean removes particles and residues by forming and dissolving hydrous oxide films.
- Ultrapure water rinse.
- Standard clean 2 (SC2): immersion of the wafer in a solution H_2O:H_2O_2 30%:HCl 37% (6:1:1) at 70-80 °C for 10 min. This removes alkali metal and hydroxides.
- Ultrapure DI water rinse and dry.

The wafer is optionally immersed in acetone and isopropyl alcohol (IPA) for several minutes before the SC1 in order to remove the possible organic contamination.

Finally it must be noted that all wafer cleaning solutions and rinses were carried out with ultrapure deionized (DI) water. DI water should be highly purified and filtered to remove all traces of ionic, particle and bacterial contamination. The water resistivity achieved by our purelab system is the maximum attainable, 18.2 MΩ cm.

As a final step all wafers were immersed in a diluted HF solution (1:50) immediately before the introduction in the ECR-PECVD or the HPS chambers in order to etch the native ~1 nm SiO_2 on the Si surface The ECR-CVD is attached to a glove box and this clean was performed in nitrogen atmosphere. This way it is

assured that the Si wafer surface is oxygen free. However, the HPS system is not provided with this kind of chamber. Thus, in order to avoid oxide regrowth, the time between the HF dip and sample loading is minimized, being in all cases less than 1 min.

II.5 Fin field effect transistor (FinFET) architecture

An important part of this thesis is devoted to the study of the reliability of bulk n-type FinFETs, which, as it was introduced in chapter I, are a strong contender to replace the traditional planar devices in the future of CMOS technology [18]. Along with this new architecture, their EOT was ultra-low, ranging from 0.8 to 0.6 nm, thanks to the TiN/HfO_x gate stack. In this section, the geometrical parameters of the studied FinFETs will be detailed.

In FinFETs the channel is not planar, but is wrapped around a silicon *fin*, which acts as the body of the device. Thus, this kind of transistors has more geometrical dimensions that must be considered when studying its performance or reliability. Several types of multi-gated transistors exist, depending on the number of sides of the fin body that are wrapped by the gate stack [19]. Also, the fin can be connected to the substrate (bulk FinFET) or it can be grown on an insulator substrate. The latter are called silicon on insulator (SOI) FinFETs [19].

This study is focused on three-gated bulk FinFETs, which present a good compromise between performance and process integration complexity [20, 21], as compared with other FinFETs architectures. In figure II.12, the FinFET device structure is depicted. The silicon fin is directly connected to the bulk, and the top and lateral surfaces of the fin body are wrapped by the gate dielectric and metal electrode. From its three-dimensional structure, the width (W_{fin}) and the height (H_{fin}) of the fin are defined as shown in figure II.12a. The distance from the gate edge to the source and drain is called fin extension (L_{ext}), as in figure II.12b. A device can contain one or multiple fins, so the number of fins (N_{fin}) and the distance between two adjacent fins or pitch (S) are parameters that have to be taken into account. Thus, the total device area A of the channel follows this expression:

$$A = (2H_{fin} + W_{fin})L_G N_{fin} \qquad \text{equation II.2}$$

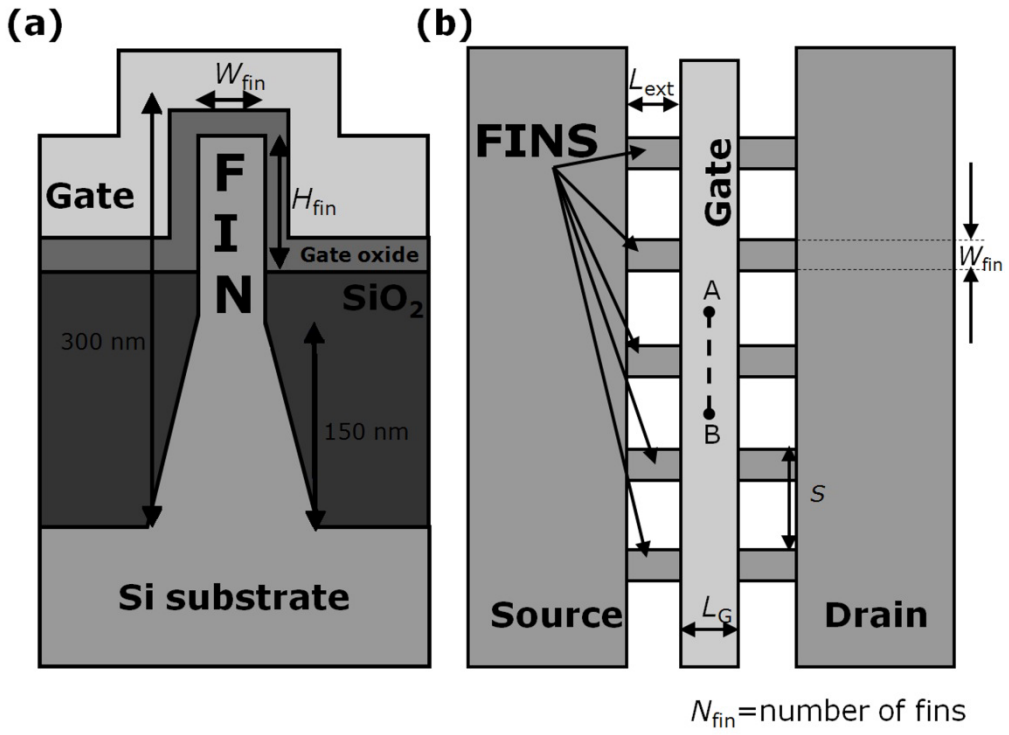


Figure II.12 (a) Schematic cross sectional view of a FinFET device. (b) Schematic top view of a FinFET consisting of five fins (cutline along A-B for fin cross-sectional view).

The n-type FinFETs were fabricated on 300 mm (100) Si wafers. The fabrication flow is detailed in references 22 and 23. It is mainly based on conventional shallow trench isolation (STI) process flow to fabricate the fins. At the beginning of the process, a typical STI stack was present (from bottom to top, Si/8 nm thermal SiO_2/70 nm CVD Si_3N_4), covered by hard mask with an antireflection layer (90 nm CVD amorphous carbon/35 nm CVD SiOC), Lithography was performed with 193 nm illumination in order to print the pattern on the carbon layer. The Si_3N_4 layer and the top straight part of the fin were patterned using $SH_2F_2/SF_6/N_2$ chemistry and the amorphous carbon layer as a mask. The sloped bottom part of the fin was etched using $Cl_2/O_2/N_2$ chemistry and the Si_3N_4 layer as a mask. The fin profiles after the trench etching are shown in figure II.13a.

After trench etching, SiO_2 was deposited by CVD, followed by a chemical mechanical polishing (CMP). Then, the field SiO_2 was recessed until the level of nitride bottom. Next, nitride was removed in a hot phosphoric bath, while fins are protected by the SiO_2. Finally, the field oxide was recessed until the desired level of fin height was attained using Siconi™ Selective Material Removal (SMR™) process

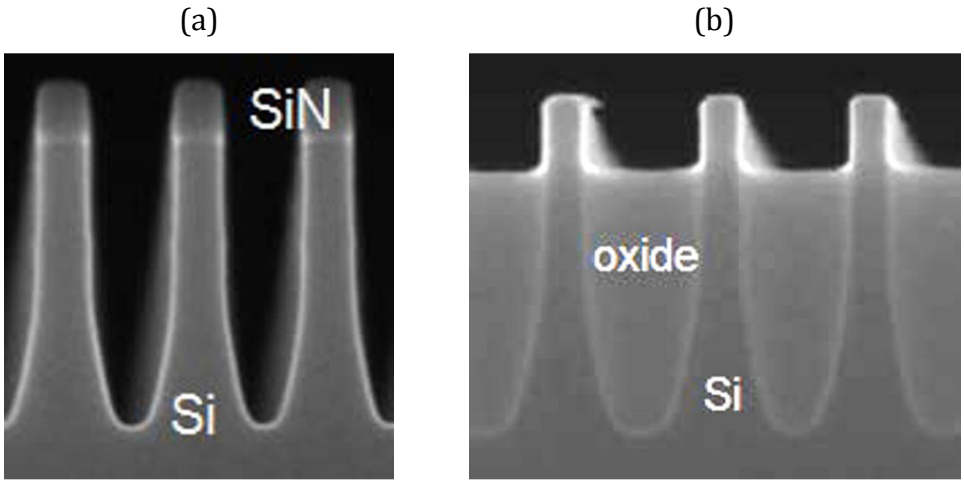


Figure II.13 (a) Trench shape after dry etching. Fin height is 280 nm and width is 35 nm. (b) Same structures after STI fabrication with trenches filled by the field oxide. Fin width is reduced to 20 nm. From reference 22.

[22]. In figure II.13b, the fin profiles are shown after the STI trench fill with oxide and subsequent recess etch.

Once the fins were produced, the 2.1 nm thick high κ HfO_x was deposited by atomic layer deposition (ALD). To reduce EOT, a thin TiN/80 nm Si-cap gate structure was used to partially scavenge the interfacial layer. The TiN electrode was deposited by physical vapor deposition (PVD). In order to achieve gate stacks with different EOTs, wafers with metal gate thicknesses of 5, 3 and 2 nm were fabricated, since it was previously observed that the reduction of the interfacial layer is more effective for the thinner TiN layers.

Chapter VIII is dedicated to the evaluation of the reliability of bulk FinFET transistors and the influence of the TiN gate. The reliability assessment techniques used in this thesis are described in next chapter.

II.6 SUMMARY

This chapter has described the experimental techniques used in sample fabrication. The HPS was thoroughly explained in section II.1 as the main deposition technique in this thesis. Then, other techniques were explained and the different fabrication flows used through this thesis were detailed. Finally, the last section of this chapter dealt with the FinFET architecture, since an important part

of this thesis consists in its reliability assessment. Next chapter will cover the characterization methods.

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CHAPTER III. CHARACTERIZATION TECHNIQUES

This chapter is divided in three parts. The section III.1 describes the electrical characterization of the metal-insulator-semiconductor (MIS) capacitors. In this way, the first sub-section begins with the analytical description of the physics of the MIS capacitor, the main device that was analyzed throughout this thesis. This is followed by the introduction to the measurement techniques that were used for the electrical characterization. The aim of Section III.2 is to give a brief explanation of the methods used for the reliability assessment of the gate stack (chapter VIII). Section III.3 concludes this chapter with the fundamentals of the structural characterization techniques, used to study the physical properties of the high κ thin films.

Along this chapter the application of the characterization techniques to the study of high κ dielectrics is considered in depth.

III.1 ELECTRICAL CHARACTERIZATION

As it was introduced in chapter I, one of the main purposes of this thesis is obtaining a high κ material with suitable properties for its application as a gate dielectric in future generations of MIS field effect devices (MISFETs). Therefore, the electrical characterization of the MIS capacitors fabricated with scandium and gadolinium oxides is essential for the determination of their suitability. These materials, as well as their ternary, could be applied in MISFET according to their electrical properties, among them, the equivalent oxide thickness (EOT), leakage current and density of interfacial traps or defects.

III.1.1 THE METAL-INSULATOR-SEMICONDUCTOR (MIS) CAPACITOR

In this sub-section, the MIS capacitor theory is explained for a better understanding of the measurement techniques [1, 2, 3].

MIS structure in equilibrium

A MIS structure consists of a metal and a semiconductor separated by an insulator. The metal corresponds to the gate of the device. The ideal case where there is no density of interfacial defects in the insulator/semiconductor interface

will be considered. The gate voltage V_G refers to the potential difference between the gate and the semiconductor, which is grounded.

In thermal equilibrium and at zero applied bias, the metal and the semiconductor Fermi levels coincide since the probability of occupation of all states with a given energy must be the same. In figure III.1a, the energy-band diagram of the MIS capacitor in equilibrium is shown. For simplicity, only the n-type semiconductor case is considered. The work-function difference ϕ_{ms} is defined as the difference between the Fermi levels of the metal and the semiconductor when they are isolated (before forming the MIS structure).

$$\phi_{ms} = \phi_m - \phi_{sc} = \phi_m - \left(\chi_{sc} + \frac{E_g}{2q} - \phi_F\right) \qquad \text{equation III.1}$$

The different magnitudes are defined as follows:

- q is the elementary charge;
- ϕ_m is the metal work function;
- ϕ_{sc} is the semiconductor work function;
- χ_{sc} is the semiconductor electron affinity;
- E_g is the semiconductor band gap;
- ϕ_F is the absolute value of the potential difference between the Fermi level and the intrinsic Fermi level E_i. It follows equation III.2.

$$\phi_F = \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \qquad \text{equation III.2}$$

In equation III.2, k_B is the Boltzmann constant, T the temperature, N_D the density of donor dopants and n_i the intrinsic density of carriers of the semiconductor.

If the semiconductor is p-type, the sign of ϕ_F must be the opposite in equation III.1, and the acceptor density N_A must replace N_D in equation III.2.

If ϕ_m is smaller than ϕ_{sc}, the metal Fermi level is above the semiconductor Fermi level. Then, to reach equilibrium some negative charge (electrons) must transfer from the metal to the semiconductor and a positive potential appears between the gate and the semiconductor. Otherwise, the electrons in the semiconductor transfer to the metal and a negative potential appears. Anyhow,

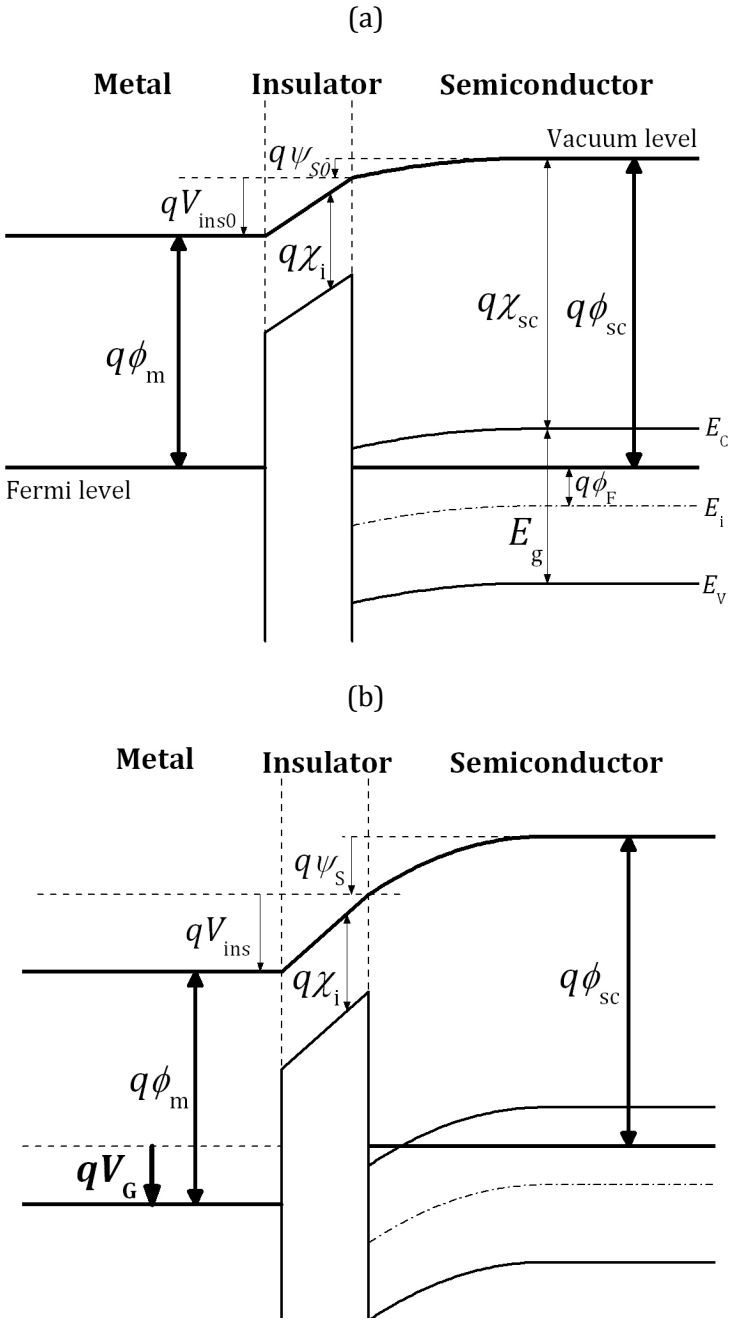


Figure III.1 Band diagram of the MIS structure in equilibrium (a) and biased (b). E_C and E_V are the semiconductor conduction and valence band respectively.

this potential is divided between the spatial charge region of the semiconductor (ψ_{S0}) and the insulator (V_{ins0}) and it compensates the work function difference as can be seen in figure III.1a.

$$\phi_{ms} = -\psi_{S0} - V_{ins0}$$ equation III.3

This result implies that, in general, when the device is not biased (V_G = 0), there is a potential drop in the semiconductor, and thus, its energy bands are bent. Energy band bending is represented as ψ_S.

MIS structure under bias

If a gate bias voltage V_G is applied, then this voltage drops across the capacitor producing a variation in the insulator voltage (V_{ins}) and the energy band bending (ψ_S) with respect to the equilibrium values (V_{ins0} and ψ_{S0}, respectively).

$$V_G = (V_{ins} - V_{ins0}) + (\psi_S - \psi_{S0}) \qquad \text{equation III.4}$$

This situation is depicted in figure III.1b. Substituting equation III.3 in equation III.4, it is concluded:

$$V_G = V_{ins} + \psi_S + \phi_{ms} \qquad \text{equation III.5}$$

Therefore, the gate voltage determines the voltage drop in the insulator and in the semiconductor and so, the energy band bending.

A very important magnitude is the flatband voltage V_{FB}. It is defined as the gate voltage necessary to achieve a flat bands in the semiconductor (in other words, no band bending, $\psi_S = 0$). In this case, the total charge in the semiconductor Q_{sc} is zero. If a charge per unit area Q_{ss} (in C/cm^2) is trapped at the semiconductor/insulator interface, V_{FB} is determined through the following relation:

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_{ins}} \qquad \text{equation III.6}$$

where C_{ins} is the insulator capacitance per unit area, which is related to the dielectric permittivity $\varepsilon_{ins} = \kappa\varepsilon_0$ and the insulator thickness t_{ins} according to the equation III.7.

$$C_{ins} = \frac{\kappa\varepsilon_0}{t_{ins}} \qquad \text{equation III.7}$$

The applied voltage V_G with respect to the flatband voltage V_{FB} defines the different operation regions of the MIS capacitor: accumulation, depletion and inversion. Figure III.2 shows the band diagram of a MIS for the three operation for the n-type semiconductor case. Fermi levels remain constant in the whole structure since in the ideal case no current flows through the device.

When the applied voltage is larger than the flatband voltage ($V_G > V_{FB}$) an excess of electrons is induced in the semiconductor close to the semiconductor/insulator interface. Then, the valence and conduction bands bend downwards ($\psi_S > 0$) and an accumulation of majority carriers is produced in the semiconductor surface. This is the *accumulation* region.

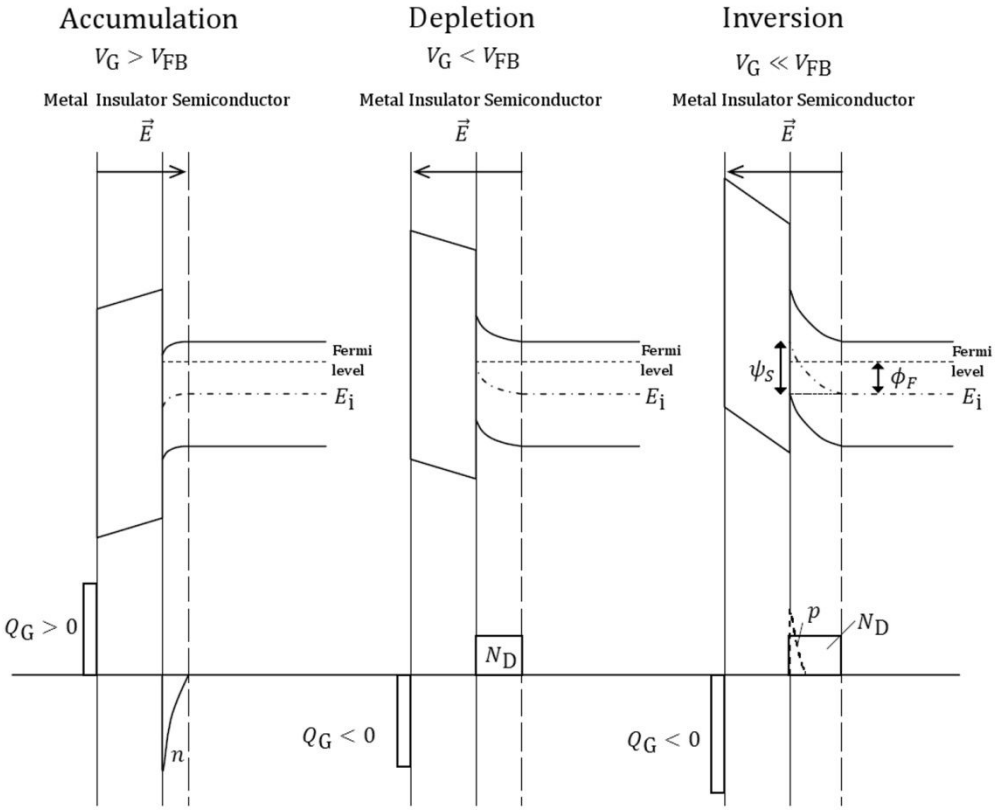


Figure III.2 Energy band diagrams (top) and charge densities (bottom) for the different operation regions of a MIS structure. $\vec{E}$ is the electric field, N_D is the donor dopant concentration, n is the density of electrons in accumulation and p is the density of holes in inversion. Q_G is the charge in the gate.

When $V_G < V_{FB}$, the energy bands bend upwards ($\psi_S < 0$), the electrons are driven away and the region closer to the insulator/semiconductor interface is depleted of majority carriers. The depletion layer presents a positive charge due to the ionized donor impurities and its width increases with decreasing gate voltage until reaching a maximum. This is the *depletion* region.

When $V_G << V_{FB}$, the energy bands bend upwards even more. The intrinsic Fermi level E_i crosses over the Fermi level ($\psi_S < -\phi_F$). Then, the voltage induces an excess of positive charges (holes) close to the interface. This is the *weak inversion* region. Finally, the *strong inversion* region is reached when the hole concentration increases exponentially for lower values of the band bending ($\psi_S < -2\phi_F$).

Similar results occur for the p-type semiconductor, reversing the polarity of the voltage.

Low and high frequency capacitance

The differential capacitance of the MIS capacitor per unit area C is defined as follows:

$$C = \frac{dQ_G}{dV_G} \qquad \text{equation III.8}$$

where Q_G is the charge in the gate per unit area. In order to measure the capacitance as a function of gate bias in the steady state, a small alternating component of voltage is superimposed to a direct current (DC) bias voltage applied to the gate. Small signal measurements determine the rate of change of charge with voltage.

The capacitance of the MIS is the series combination of the semiconductor capacitance C_S and the insulator capacitance C_{ins} as can be observed in the equivalent circuit represented in figure III.3a. C_S is modeled as a variable capacitance since it depends on the band bending ψ_S and thus, on the gate voltage V_G. Therefore, the total capacitance depends on the gate voltage.

The semiconductor response also depends on the frequency f of the alternating current, and two cases are commonly distinguished: low frequency (LF) and high frequency (HF). The associated capacitances are represented as $C_{LF}(V_G)$ and $C_{HF}(V_G)$, respectively. The total capacitance C is then determined by equation III.9.

$$\frac{1}{C(V_G,f)} = \frac{1}{C_{ins}} + \frac{1}{C_S(V_G,f)} \qquad \text{equation III.9}$$

Figure III.3b shows the total capacitance of an ideal MIS capacitor with n-type semiconductor for low and high frequency. Starting from accumulation, a high capacitance can be observed. This is caused by the high number of electrons accumulated in the semiconductor surface. The total capacitance is then close to the insulator capacitance C_{ins}. As the gate voltage is reduced under V_{FB}, the depletion layer appears and acts as an insulator in series, so the total capacitance decreases. In low frecuencies the capacitance presents a minimum and then increases again as the inversion layer of holes forms at the surface. The increase of the capacitance depends on the ability of the minority carrier concentration to follow the applied alternating signal. This only happens at low frequencies where the recombination-generation rates of minority carriers can keep up with the small signal variation. At high frequencies the minority carriers cannot follow the

alternating signal, and as a result, C-V_G curves measured at frequencies larger than ~100 Hz do not show the increase of the capacitance in the inversion region.

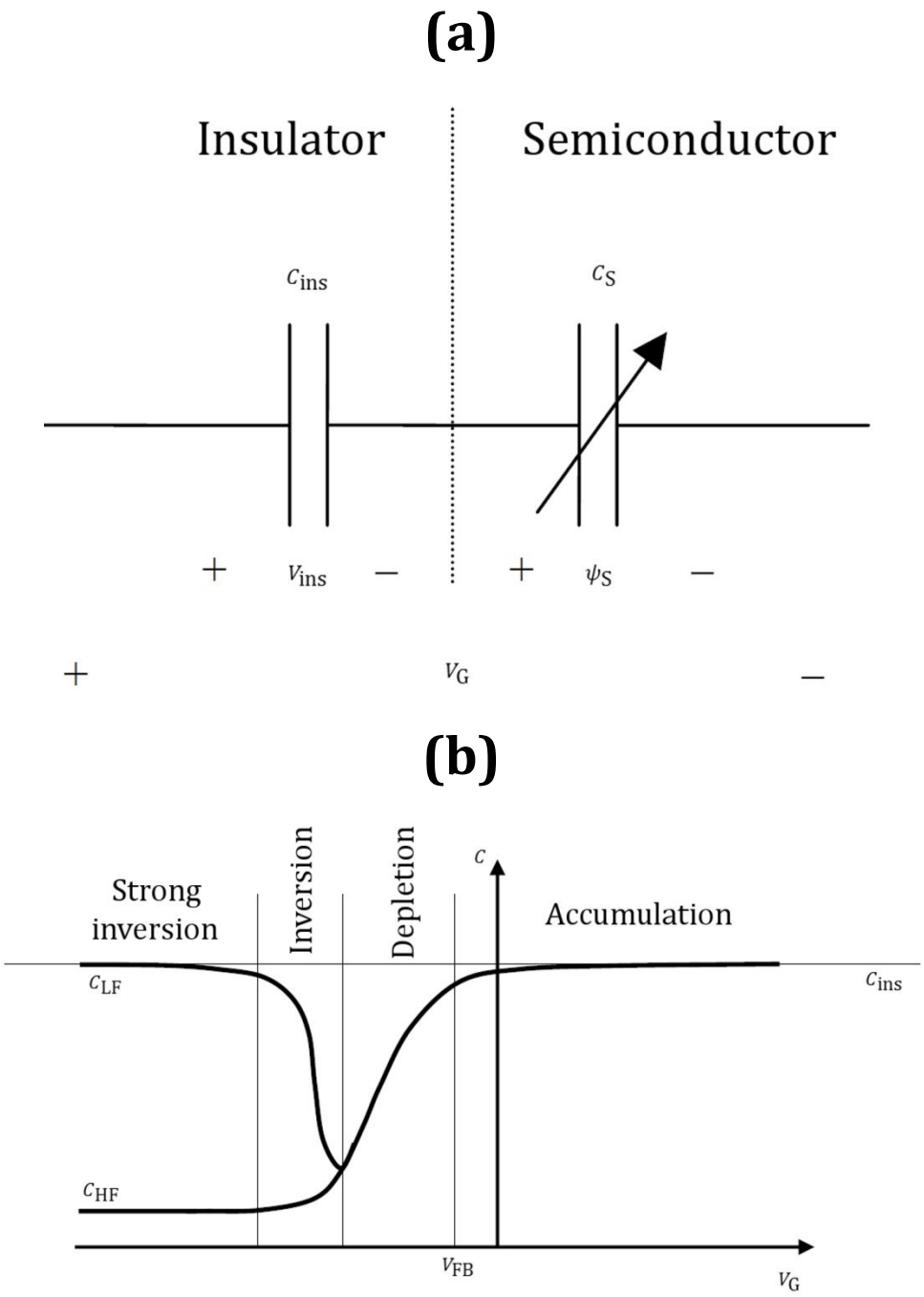


Figure III.3 (a) Small signal equivalent circuit of an ideal MIS capacitor. (b) C-V_G characteristics at high frequency (HF) and low frequency (LF) for an n-type semiconductor.

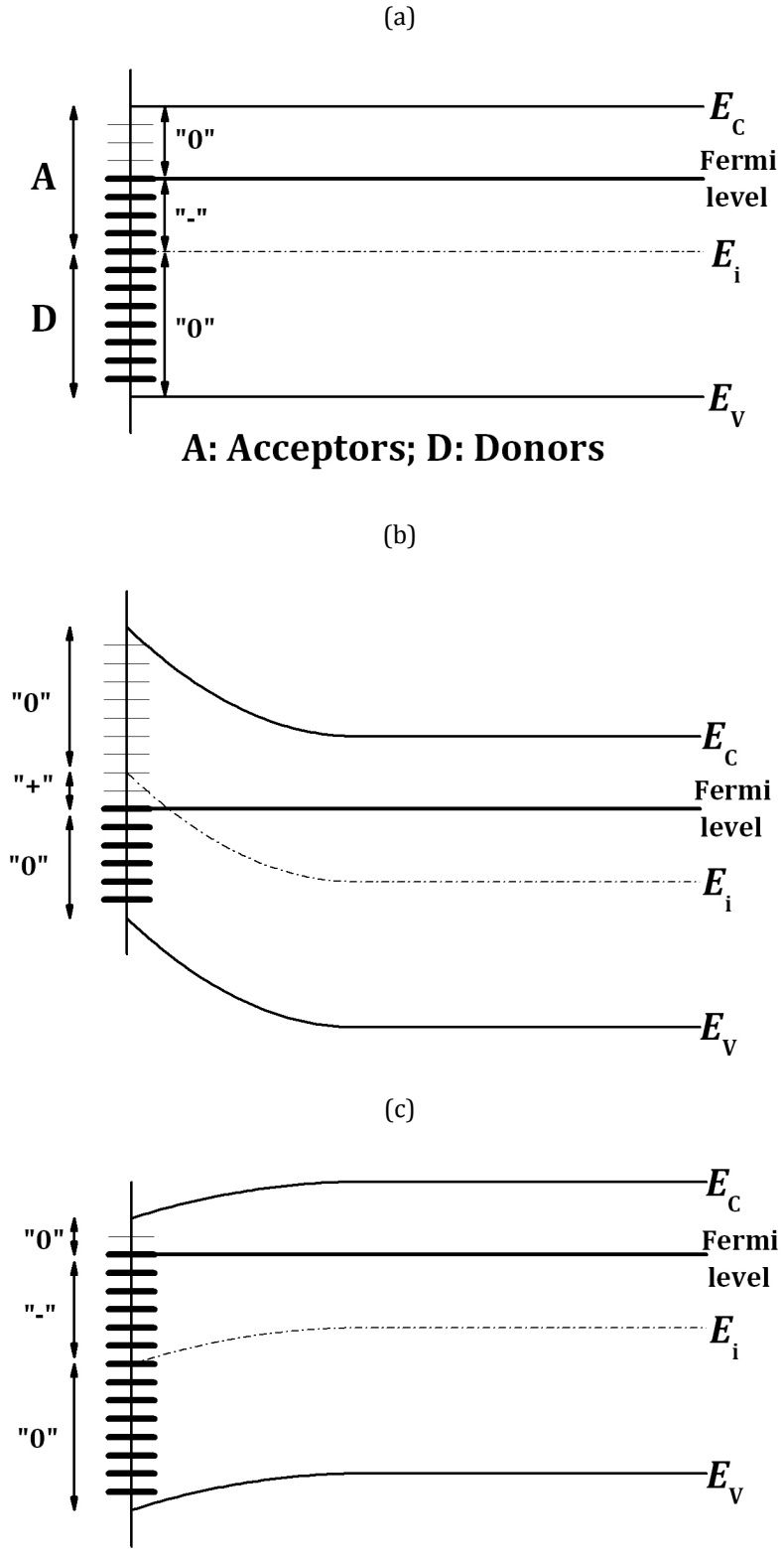


Figure III.4 Occupancy of interface states as a function of the band bending for a n-type semiconductor. (a) $\psi_S = 0$, (b) $\psi_S < 0$, (c) $\psi_S > 0$. Occupied traps are indicated by the small horizontal heavy lines and the unoccupied traps by the light lines.

Flatband voltage determination

The determination of the flatband voltage V_{FB} was very important throughout this thesis. Its calculation was useful for assessing the charges in the oxide caused by different processes. The V_{FB} is measured from the gate bias that corresponds to a calculated flatband capacitance C_{FB} on a C_{HF}-V_G curve. This method is widely used because of its simplicity. To compute C_{FB}, equation III.9 must be used with $C_S = \varepsilon_S / L_D$, where ε_S is the dielectric permittivity of the semiconductor and L_D the Debye length. L_D can be seen as the penetration length of the electric field in the semiconductor at flatband conditions and it is calculated for n-type semiconductors according to equation III.10.

$$L_D = \sqrt{\frac{k_B T \varepsilon_S}{q^2 N_D}} \qquad \text{equation III.10}$$

For p-type, N_D must be replaced for N_A.

In the above discussion, the effect of the charge trapping in the insulator/semiconductor interface was neglected. However, the influence of the interface traps on the capacitance of the MIS is described in the following sub-section.

III.1.2 INTERFACE DEFECTS IN THE STACK

The semiconductor/insulator interface presents energy levels within the gap of the semiconductor. These charge traps are usually attributed to dangling bonds at the interface and they have a distribution $D_{it}(E)$ over the band gap. Q_{it} represents the charge per unit area that is trapped at the interface because of these energy levels, and its value depends on the band bending. The interface traps are usually passivated with hydrogen by a forming gas anneal at moderate temperatures (300 - 450 °C) performed as the final step of the integrated circuit fabrication.

The most common model that explains the nature of the traps attributes donor-like behavior to the energy levels below the intrinsic energy level E_i and acceptor-like behavior to the D_{it} above E_i, as is observed in figure III.4a for a n-type semiconductor [4, 5]. Their occupancy depends on the band bending. The donor traps below the Fermi level are occupied by electrons and hence they remain neutral. Likewise, the acceptor traps above the Fermi level are empty states and then they also remain neutral. Acceptor interface levels with energies between the

Fermi level and the intrinsic level E_i are occupied states and thus they involve a net negative charge. Donor traps with energies between the Fermi level and E_i are unoccupied states and involve a positive charge. Therefore, the capacitance curves shift to the left for small gate voltages, and to the right for high gate voltages. Both curves coincide when Q_{it} equals zero, that is, when $-\psi_S = \phi_F$ for a n-type semiconductor ($\psi_S = \phi_F$ for an p-type). A comparison between a C_{HF}-V_G curve with a density of states and one without is depicted in figure III.5. In the figure, it is assumed that the interface traps do not contribute to the total capacitance since they cannot follow the high frequency signal. However, interface traps can follow the slowly varying gate bias.

The different methods used through this work to estimate the density of interfacial defects are explained in this sub-section.

Quasi-static method

The interface trap level density D_{it} can be measured by comparison of the high frequency capacitance C_{HF} with the low frequency or quasi-static capacitance C_{LF}. This method was introduced by Berglund [6] and simplified by Castagné and Vapaille [7].

The high frequency capacitance must be determined at a frequency where the interface traps are assumed not to respond. On the other hand, low frequency means that the interface traps and the minority carriers must be able to respond.

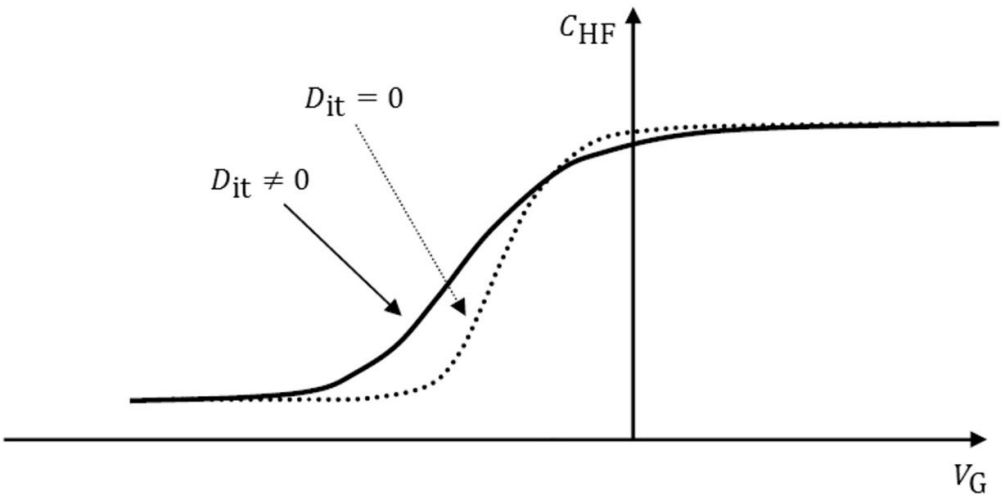


Figure III.5 Stretching out of the C_{HF}-V_G curve due to the charge trapping in the insulator/semiconductor interface.

At this low frequency, the interface states contribute a capacitance C_{it} in parallel with the capacitance of the depletion layer in the semiconductor C_S. The equivalent circuit is depicted in figure III.6. The total capacitance at low frequency is then:

$$C_{LF} = \left(\frac{1}{C_{ins}} + \frac{1}{C_S + C_{it}}\right)^{-1} \qquad \text{equation III.11}$$

For high frequencies, the interface states do not contribute ($C_{it} = 0$) and the capacitance is:

$$C_{HF} = \left(\frac{1}{C_{ins}} + \frac{1}{C_S}\right)^{-1} \qquad \text{equation III.12}$$

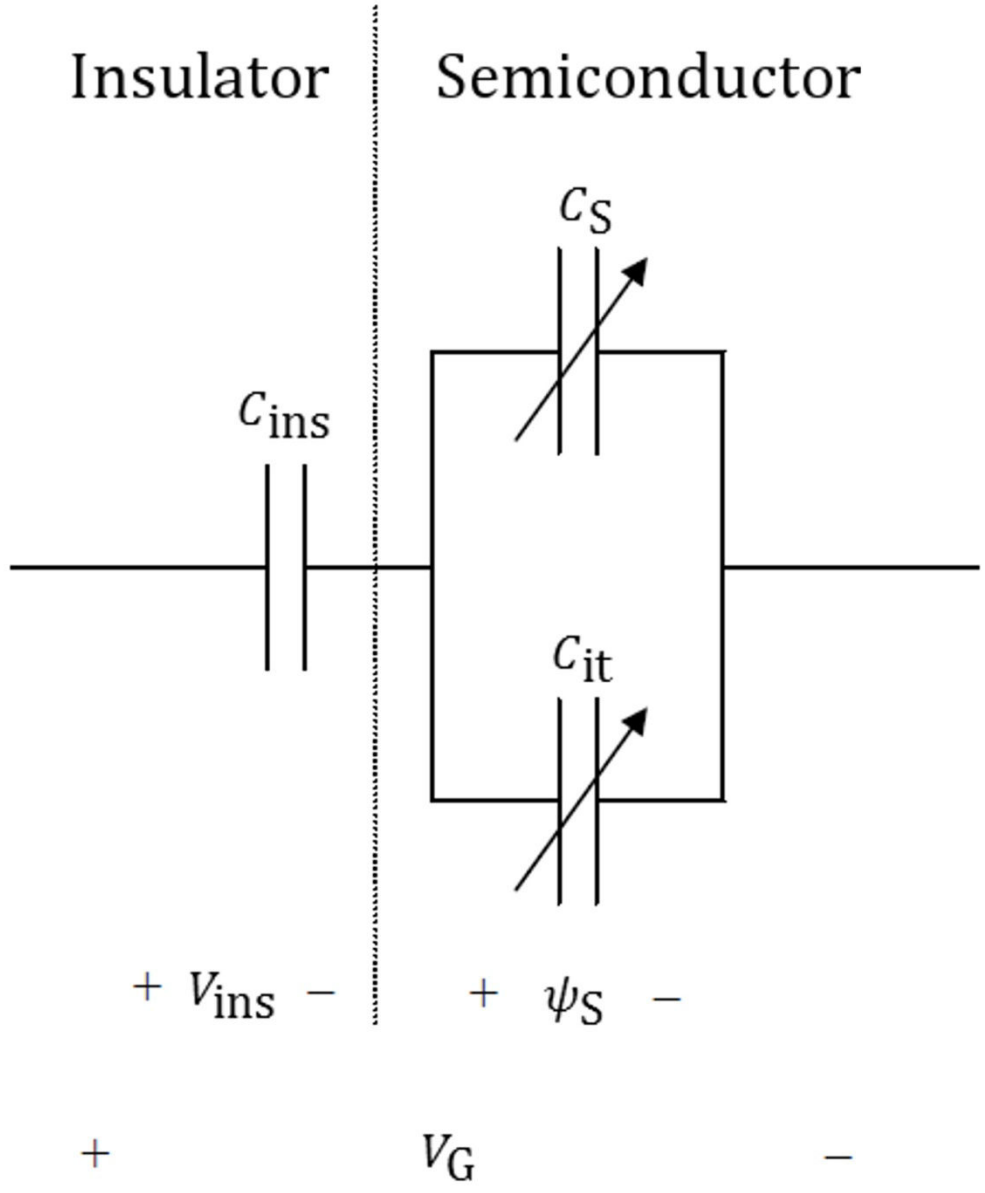


Figure III.6 Small signal equivalent circuit of a MIS capacitor with the contribution of D_{it}.

The interface capacitance C_{it} is related to the interface trap density D_{it} by equation III.13.

$$D_{it} = \frac{C_{it}}{q^2} \qquad \text{equation III.13}$$

Substituting equation III.12 into equation III.11 and using equation III.13, the D_{it} is determined by the HF and LF capacitance curves as

$$D_{it} = \frac{1}{q^2}\left(\frac{C_{ins}C_{LF}}{C_{ins}-C_{LF}} - \frac{C_{ins}C_{HF}}{C_{ins}-C_{HF}}\right) \qquad \text{equation III.14}$$

Equation III.14 gives the interface trap density for each value of V_G. However, it is only valid over a limited range of the band gap, typically from the onset of inversion to a surface potential towards the majority carrier band at about 0.2 eV from that band [3]. The C_{ins} can be extracted from the capacitance measured in accumulation.

Finally, the position of the Fermi level inside the semiconductor gap as a function of the gate voltage must be determined to obtain the interface trap density as a function of the energy level D_{it} (E). The band bending can be calculated from the C_{LF}-V_G curve using equation III.15. The trap energy E_{it} with respect to the conduction band edge E_C is related to the band bending ψ_S by the equation III.16 (ref. 6).

$$\psi_S(V_G) = \int_{V_{FB}}^{V_G}\left(1 - \frac{C_{LF}(V_G')}{C_{ins}}\right)dV_G' \qquad \text{equation III.15}$$

$$E_C - E_{it} = \frac{E_g}{2} - q\psi_S - q\phi_F \qquad \text{equation III.16}$$

Equation III.16 is valid only for n-type semiconductor. For p-type, the sign of $q\phi_F$ must be opposite.

In this thesis, the measurement of HF and LF capacitance curves was carried out by a *Keithley Model 82* system, which consists of a voltage source, a *C-V* analyzer, a quasi-static *C-V* meter and a remote input coupler. They were all controlled by the *Metrics ICS 7.0* software. To measure the C_{HF}-V_G curve, an alternating voltage of 30 mV of 100 kHz was superimposed on the gate bias V_G. The quasi-static curve (C_{LF}-V_G) was calculated by applying a voltage step ΔV_G and measuring the displacement charge ΔQ. The quasi-static capacitance is the quotient of ΔQ and ΔV_G. With the usual step ΔV_G of 20 mV and a delay time of 0.07 s, the leakage current through the device must be lower than 0.3 nA for

accurate C_{LF}-V_G measurements [1]. This means that the insulator must be relatively thick and defect-free in order to use this technique.

Figure III.7 shows a typical C_{HF}-V_G and C_{LF}-V_G characteristics of a MIS device with a Sc_2O_3 as gate dielectric and the D_{it} extracted with this method.

Conductance method

The conductance method is one of the most sensitive methods to determine D_{it}. It was proposed by Nicollian and Brews in 1967 [1]. This method consists in extracting D_{it} from the admittance in depletion ($Y_m = G_m + i\,\omega C_m$), measured as a function of the gate voltage V_G and the frequency $\omega = 2\,\pi f$. When there is no gate leakage, the conductance G_m is due to the interface trap density since it represents the loss mechanism from interface trap capture and emission of carriers. The following paragraphs give a qualitative description of the energy loss caused by a small alternate current signal superimposed on the gate bias V_G.

Following Nicollian and Brews [1], the interface trap levels change their occupancy due to the small variations of gate voltage. In the positive half cycle of the signal the conduction band approaches the Fermi level at the Si surface. The average energy of the electrons of the conduction band immediately increases. At

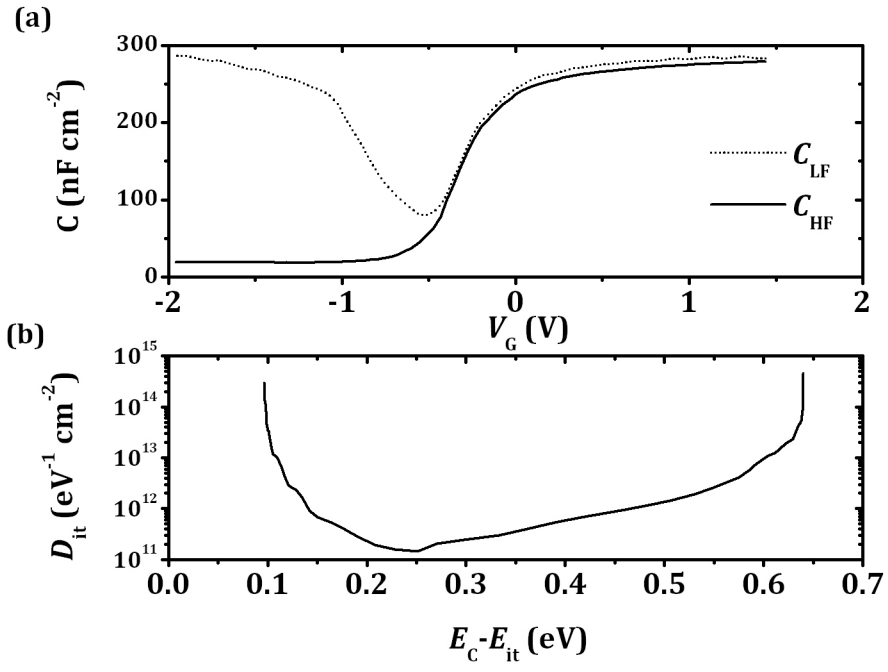


Figure III.7 (a) C_{HF}-V_G and C_{LF}-V_G characteristics of a MIS device. (b) Density of states as a function of the energy level obtained by the quasi-static method.

frequencies where an energy loss is observed, interface traps do not respond immediately but lag behind the alternate gate voltage. Thus there are empty interface trap levels below the Fermi level in the Si. An energy loss occurs when electrons at a higher average energy in the Si are captured by interface trap levels at a lower average energy, eventually making the average energy of trapped electrons the same as that of the free electrons. The energy lost during electron capture is taken up by phonons, heating the lattice.

In the negative half cycle, the conduction band moves away from the Fermi level at the Si surface. Electrons in filled interface trap levels above the Fermi level in the Si will be at a higher average energy than electrons in the Si. As electrons are emitted by interface traps into the Si, the electrons lose energy again until the energy of trapped electrons becomes equal to that of the free electrons. The energy needed to emit electrons from interface trap levels to the Si conduction band is provided by phonons. Emitted electrons enter the high energy tail of the Fermi distribution, raising the average energy of electrons in the Si momentarily. The ensemble of electrons in the Si then returns to its original average energy through phonons, heating the lattice

Therefore, there is energy loss in both halves of the cycle that must be supplied by the signal source. This energy loss is modeled as a conductance G_P in parallel with the capacitance of the semiconductor C_S and the capacitance of the interface states C_{it}. Then, the equivalent circuit for a MOS structure is shown in figure III.8a.

To determine the D_{it} distribution, the admittance of the MIS device is measured as a function of V_G and ω, obtaining G_m and C_m, as the equivalent circuit in figure III.8b. The equivalent parallel conductance G_P is related to the measured G_m and C_m according to equation III.17. The insulator capacitance C_{ins} is determined from the admittance in strong accumulation.

$$\frac{G_P}{\omega} = \frac{\omega C_{ins}^2 G_m}{G_m^2 + \omega^2 (C_{ins} - C_m)^2}$$ equation III.17

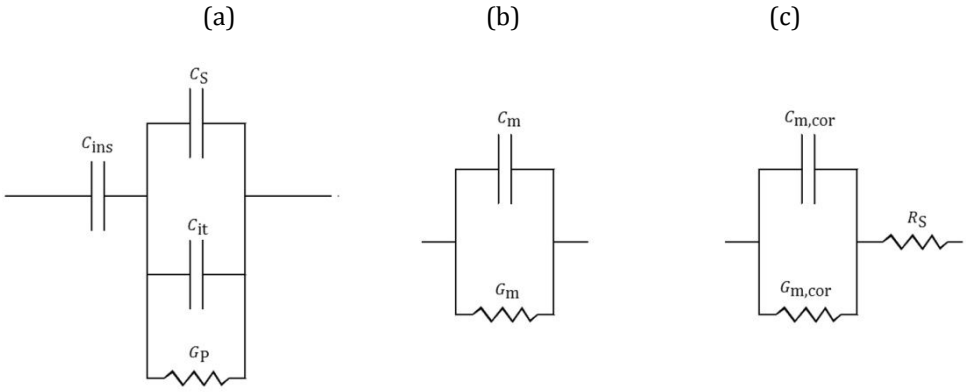


Figure III.8 (a) Small signal equivalent circuit of a MIS capacitor with a contribution of D_{it} to capacitance and energy loss. (b) Measured admittance of the device. (c) Corrected admittance with the series resistance R_S.

The density of interfacial traps D_{it} is evaluated by means of equation III.18 where $(G_P/\omega)_{max}$ is the maximum of equation III.17 as a function of the frequency ω and gate voltage V_G [1, 3], where G_P is in S (Ω^{-1}) per unit area.

$$D_{it} = \frac{1}{0.4\,q^2}\left(\frac{G_P}{\omega}\right)_{max} \qquad \text{equation III.18}$$

In a simplification proposed by Hill and Coleman, a single C_m–V_G and G_m–V_G curve at a high frequency is enough to give an estimation of D_{it} [8].

Nonetheless, a series resistance R_S can cause large distortions in the measurement of the conductance G_m and therefore, in the extraction of the density of interfacial traps. Figure III.8c depicts the equivalent circuit with the series resistance. The largest effect of R_S takes place in strong accumulation. The series resistance R_S can be calculated at strong accumulation from the capacitance C_{ma} and parallel conductance G_{ma}. The measured capacitance C_m and conductance G_m are corrected in all the range of V_G according to the following equations.

$$R_S = \frac{G_{ma}}{G_{ma}^2+\omega^2 C_{ma}^2} \qquad \text{equation III.19}$$

$$C_{m,cor} = \frac{G_m^2+\omega^2 C_m^2}{a^2+\omega^2 C_m^2} C_m \qquad \text{equation III.20}$$

$$G_{m,cor} = \frac{G_m^2+\omega^2 C_m^2}{a^2+\omega^2 C_m^2} a \qquad \text{equation III.21}$$

$$a = G_m - R_S(G_m^2 + \omega^2 C_m^2) \qquad \text{equation III.22}$$

Capacitance and conductance measurements as a function of gate voltage and frequency were carried out by means of an *Agilent 4294A* impedance analyzer. Figure III.9 shows a typical C_m and G_m measurement at 100 kHz before and after the correction of the influence of the series resistance.

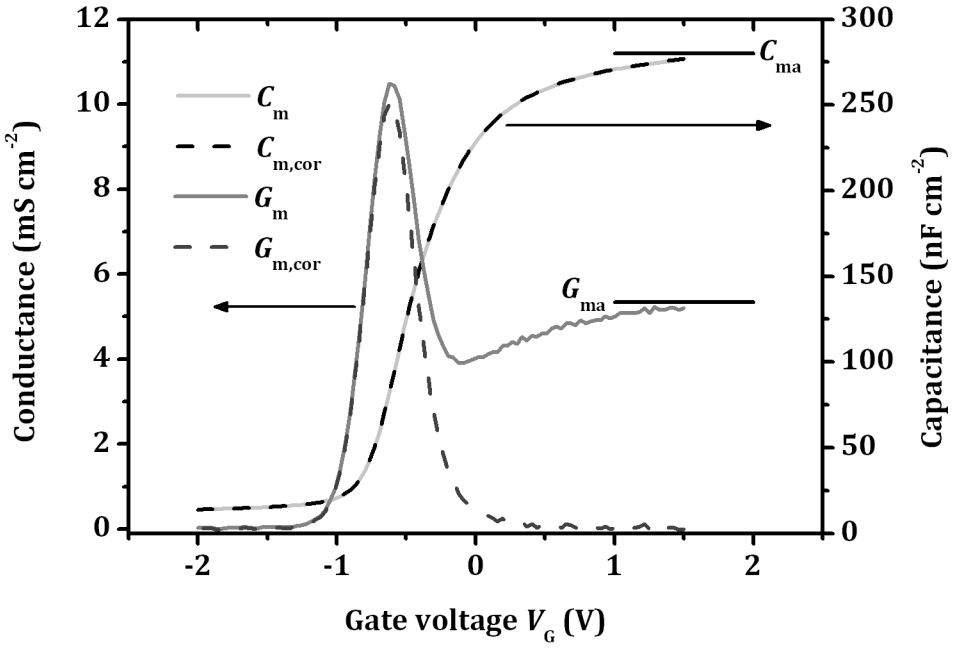


Figure III.9 C_{HF}-V_G and G-V_G characteristics of a MIS device before and after R_S correction.

Charge pumping method

This technique was proposed by Brugler and Jespers in 1969 [9] for D_{it} determination in Si metal-oxide-semiconductor field-effect-transistors (MOSFET). This method consists in applying a pulse train with sufficient amplitude for the substrate to be driven into inversion and accumulation. It cannot be used in MIS capacitors since a minority carrier source is needed to allow the semiconductor surface to be quickly driven into inversion. In MISFETs, the source and the drain of the transistor act like this minority carrier source. The pulse train prompts a current I_{cp} that is proportional to D_{it} due to the charge trapping and detrapping of the interface defects during the transitions from inversion to accumulation and from accumulation to inversion. The charge pumping current follows equation III.23, where f is the frequency of the pulse train and A is the area of the capacitor.

$$I_{cp} = qfAN_{it} = qfA \int D_{it}(E)\, dE \qquad \text{equation III.23}$$

In this thesis, the charge pumping method was used to evaluate the number of defects N_{it} in FinFETs and to discuss about its influence on the reliability.

Charge trapping: hysteresis

The applied gate voltage can inject carriers from the semiconductor to the insulator. Injected carriers have the opposite sign of the applied voltage. Then, if the gate voltage is positive, the injected carriers are electrons. Likewise, injected carriers are holes for negative voltages. These carriers can be trapped in slow states inside the dielectric or at the insulator/semiconductor interface. According to equation III.6, this extra charge changes the insulator charge and prompts a shift in V_{FB}.

When measuring the C_{HF}-V_G curves from inversion to accumulation and then from accumulation to inversion, when these slow traps are present, a hysteresis cycle is found due to the charge trapping effect. In the case of an n-type semiconductor, accumulation occurs for positive voltages, so the V_{FB} shifts towards higher voltages. A higher density of defects increases the probability of charge trapping.

Throughout this thesis, the hysteresis measurement has proved to be a useful tool for insulator assessment. Dielectrics with high densities of defects present high V_{FB} shifts while good quality dielectrics do not have hysteresis. A typical hysteresis C_{HF}-V_G curve of an scandium oxide device is represented in figure III.10, where a high ΔV_{FB} was found.

III.1.3 LEAKAGE CURRENT

The current that flows through the MIS capacitor when it is biased produces extra energy consumption that must be minimized. The International Technology Roadmap for Semiconductors (ITRS) projects maximum leakage current densities J_G of 100-200 A cm^{-2} for both high performance (HP) and low operating power (LOP) devices at 100 °C and gate voltages of 1 V in the next generations of Si devices [10]. In fact, as it was introduced in chapter I, the main purpose of the high κ dielectrics is to substitute the traditional silicon oxide with a thicker layer with higher permittivity to increase the areal gate capacitance while reducing the gate leakage current.

In this thesis the density currents were mainly measured in accumulation. This situation allows the characterization of the dielectric exclusively, since almost

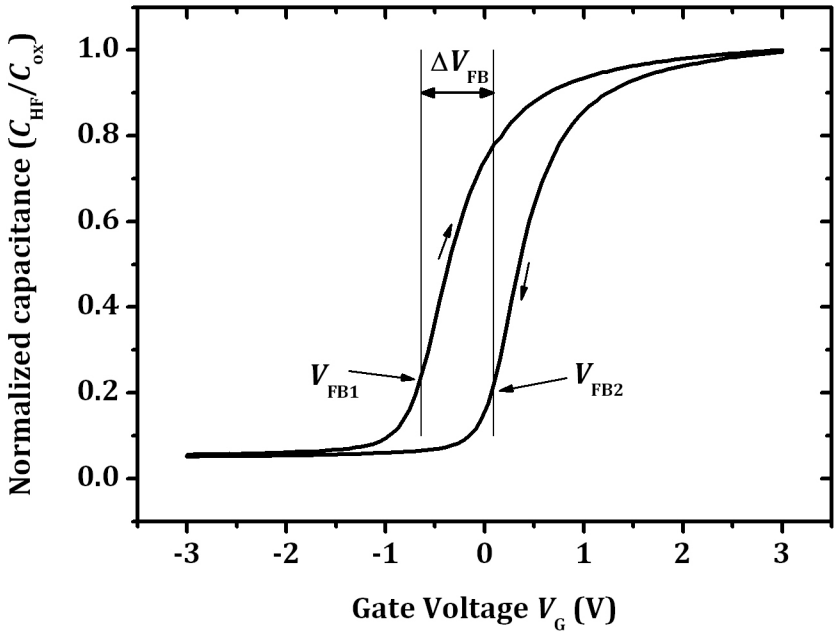


Figure III.10 Hysteresis C_{HF}-V_G curve of a MIS device.

no electric field penetrates into the semiconductor. In depletion or inversion polarizations, the depletion layer contributes to the insulation, so the leakage currents are lower.

The J_G-V_G measurements were carried out by means of a *Keithley 2636A* System, controlled by Labview software. This equipment can work simultaneously as a voltage source and an ammeter. An example of a J_G-V_G curve of a Pt/8 nm $GdScO_3$/n-Si device can be observed in figure III.11.

III.2 RELIABILITY ASSESSMENT

Gate dielectric degrades because of the operation conditions and, as the heart of the MISFET transistor, this degradation reduces drastically device performance. The generation of defects in the dielectric and the charge that can be trapped can lead to a complete failure of the transistor. It is thus vital to study the reliability in order to guarantee correct operation during the required lifetime.

Moreover, the scaling of transistors to EOTs below 1 nm, with the introduction of high κ dielectrics and new three-dimensional architectures, raises new questions about reliability [11]. Chapter VIII deals with time-dependent dielectric breakdown (TDDB) and bias temperature instabilities (BTI) of n-channel

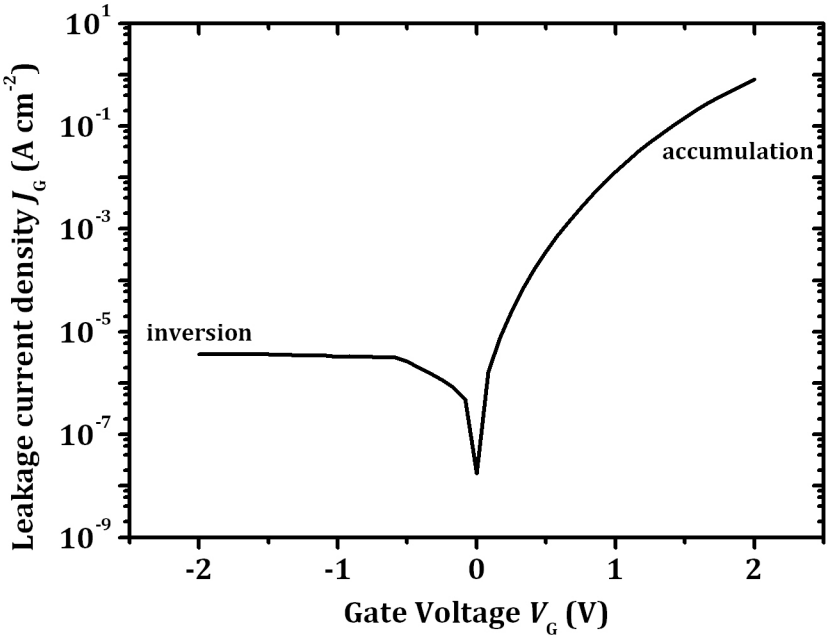


Figure III.11 J_G-V_G characteristic of a n-type MIS device.

bulk FinFETS with EOTs below 1 nm. This section describes these reliability issues and their assessment procedure. The devices were fabricated and the measurements were carried out at Imec (Leuven, Belgium).

III.2.1 TIME-DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

Dielectric breakdown is one of the main reliability issues in modern CMOS devices [12, 13]. When a voltage is applied to the gate of a transistor, the electric field generates defects in the dielectric that act like electron traps. Because of the electrical stress, the amount of generated traps increases and they eventually form a percolation path [14]. The number of traps needed to form a percolation path depends on the trap effective radius *r* and the insulator thickness, as can be seen in figure III.12a for a dielectric between two electrodes.

TDDB Measurement procedure

The most commonly used method to determine the time-to-breakdown of a MOS structure is the *constant voltage stress* (CVS). In CVS, a constant voltage V_G is applied to the gate and the gate current I_G is measured versus time. Source, drain and substrate are grounded during measurement. A typical I_G-t curve can be observed in figure III.12b. Created traps result in an increase on the gate current,

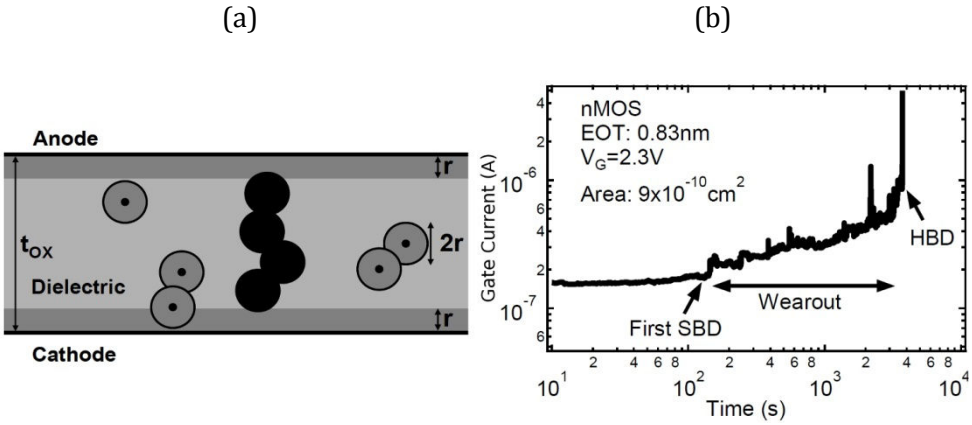


Figure III.12 (a) Defects in the dielectric created during electrical stress. If a percolation path is formed, breakdown occurs. From reference 12. (b) Gate current as a function of time for a CVS. The SBD occurs at 150 s, initiaing the wearout phase of multiple SDBs and enhanced localized degradation. The dielectric loses its isolating properties when HDB is formed. From reference 13.

and degradation presents several phases, which are explained in the following paragraphs.

Initially, there are few defects in the unstressed dielectric and the conduction mechanism is tunneling. After stress, single defects are created and they can act as traps and produce a small increase in the current [15]. Continuous stress keeps on increasing the number of traps in the dielectric, increasing the probability of creating a percolation path. Such multiple-trap conduction path carries currents much larger than a single trap path. The value of these currents strongly depends on the dielectric thickness, temperature, gate voltage and the location of the trap [16, 17]. The apparition of the first percolation path indicates *soft breakdown* (SBD). Local currents along conduction paths lead to accelerated degradation. More defects are created along the conduction path, resulting in a growth and *wearout* of the breakdown spot. The current increase contributes to a positive feedback mechanism that enhances trap generation and increases current and noise. Eventually, the dielectric loses its insulating properties and the current increases up to the compliance of the measurement set-up. This is known as *hard breakdown* (HBD).

In order to evaluate TDDB in a FinFET device, I_G-t traces must be measured in a large set of identical devices for several gate voltages. To assess reliability at the worst-case scenario, the temperature is maintained at 125 °C. In figure III.13a, it

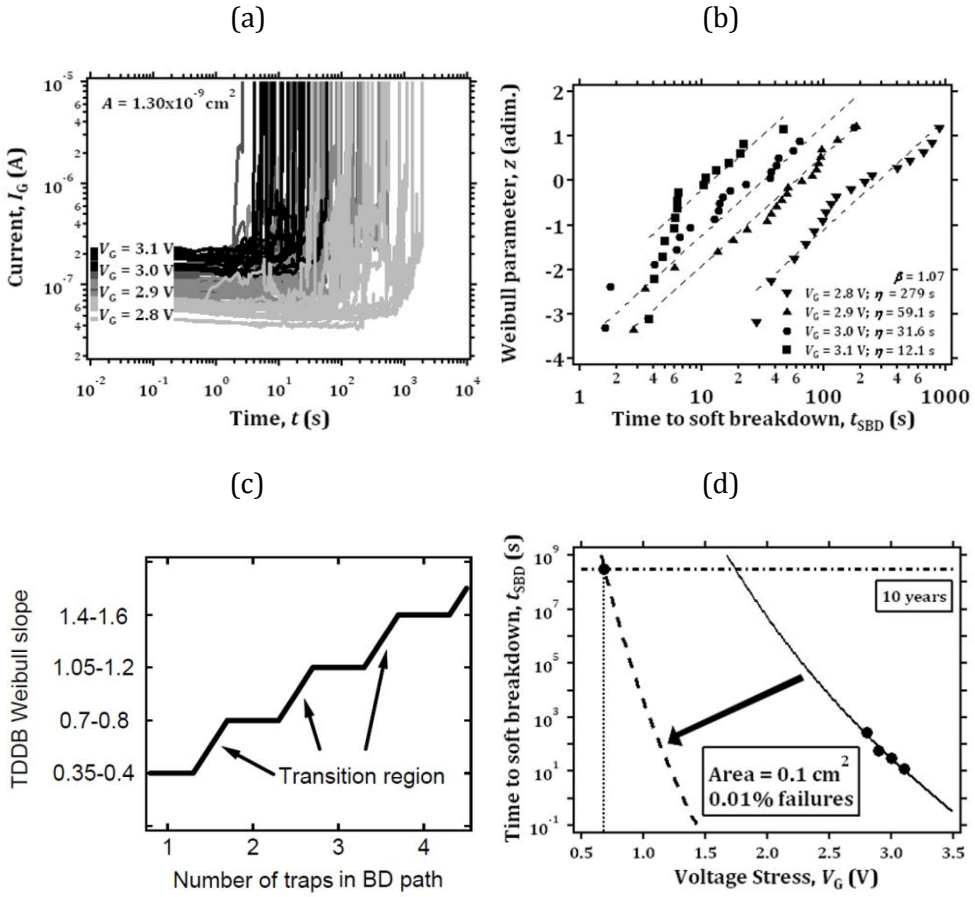


Figure III.13 (a) I_G-t traces measured on a 0.8 nm EOT n-type FinFET for several stress voltages. (b)This Weibull plot is created by ranking the t_{SBD} data using the Benard approximation and plotting the Weibit versus the time-to-breakdown. (c) The t_{SDB} Weibull slope β as a function of the number of traps involved in a percolation path. From reference 12. (d) Exponential fit through the time-to-breakdown values towards lower voltage values. To obtain the lifetime and the stress voltage at 10 years according to the TDDB reliability specification, t_{SBD} must be scaled to an area of 0.1 cm^2 and 0.01% failure probability.

can be observed a set of I_G-t curves for a specific wafer. Then, the time to SBD t_{SBD} must be calculated for each curve by selecting a current step trigger. The value of the current step trigger has to be the current of a single percolation path.

TDDB data analysis

The set of t_{SBD} values from identical measurements must be treated statistically. The time to failure or t_{SBD} is assumed to follow the Weibull distribution, which is widely used in failure analysis of materials under external stress. It was first applied to TDDB by Hill in 1983 [18]. For this work, it can be expressed as:

$$F(t_{SBD}) = 1 - \exp\left[-\left(\frac{t_{SBD}}{\eta}\right)^{\beta}\right]$$ equation III.24

where F is the cumulative distribution function and β and η are the parameters of the Weibull distribution function. The value of $F(t_{SBD})$ represents the probability that a device will fail at or before t_{SBD} and takes values from 0 to 1. The parameter β is called Weibull slope and η is the time for which 63% of the devices have failed.

In order to extract the Weibull parameters (β and η) from a fit of the measured set of t_{SBD}, the empirical cumulative distribution function is represented in a special plot that is called Weibull plot. The axes of the Weibull plot are the logarithm of t_{SBD} and the Weibull parameter z, defined in equation III.25.

$$z = \ln[-\ln(1 - F)]$$ equation III.25

The reason for this change of variables is the linearization of the graph. Therefore, if the t_{SBD} data is represented then a straight line is expected on a Weibull plot, where the slope is β and the z-intercept is -$\beta \ln \eta$, according to equation III.26.

$$z = \beta(\ln t_{SBD} - \ln \eta)$$ equation III.26

To estimate the cumulative distribution function $F(t_{SBD})$, the measured set of t_{SBD} is sorted from smallest to largest and then the Bernard approximation is used:

$$F(i) = \frac{i-0.3}{N+0.4}$$ equation III.27

where i is the number of the failed device and N is the total number of tested devices. Figure III.13b shows four separate Weibull distributions, using the t_{SBD} data and equations III.27 and III.25. The measurements were done on the same device for different stress voltages.

In figure III.13b, the data are fitted by the Maximum Likelihood Estimation method, obtaining a η for each gate stress and a Weibull slope β for all sets. For an intrinsic failure distribution, β is related to the number of traps that form a percolation path through the dielectric [19]. This relation is showed in figure III.13c.

Lifetime extrapolation

Lifetime extrapolation methods must be used in order to predict the lifetime at low operation voltage based on the t_{SDB} distributions measured at higher voltages. An exponential dependence of the time-to-soft-breakdown was

demonstrated to be valid for SiON and high κ dielectrics [20, 19]. Then, the parameter η follows equation III.28, where B is a constant and γ is the acceleration factor.

$$\eta = BV_G^{-\gamma} \qquad \text{equation III.28}$$

Figure III.13d shows the graphical representation of the time-to-failure η versus the gate voltage V_G and the extrapolation towards lower voltages. However, this fit is only valid for 63% of failures and the area of the tested devices (1.30×10^{-9} cm^2 in this case). For a TDDB lifetime extrapolation the fit still has to be scaled according to the reliability specifications which are typically at 0.01% failures for a total gate oxide area of 0.1 cm^2 [21].

To scale the area, it must be assumed that breakdown occurs at random positions across the device. Then it is possible to calculate the corresponding time-to-soft-breakdown of the 63% of devices η_2 for an area A_2 if η_1 and β have been measured for an area A_1, using the area scaling effect [22]:

$$\eta_2 = \left(\frac{A_1}{A_2}\right)^{\frac{1}{\beta}} \eta_1 \qquad \text{equation III.29}$$

For the final lifetime extrapolation at 0.01% failures $t_{0.01\%}$, that is, the dashed line in figure III.13d, equation III.30 must be applied, with F = 0.01% = 0.0001.

$$t_{0.01\%} = \eta[-\ln(1-F)]^{\frac{1}{\beta}} \qquad \text{equation III.30}$$

The figure of merit that is commonly accepted is the extrapolated operation voltage at 10 years lifetime, extracted as can be seen in figure III.13d. It should be compared with the ITRS requirements of below 0.9 V of supply voltage for the next generations of silicon devices [10].

III.2.2 Bias Temperature Instabilities (BTI)

Bias temperature instabilities (BTI) is a phenomenon that occurs in MISFET devices and is observed as an increase in the absolute threshold voltage under the influence of an applied gate voltage stress at elevated temperature [23]. This threshold voltage shift prompts a degradation in mobility, drain current, and transconductance of the transistor. The p-channel MISFET transistors usually operate with negative gate voltage, thus this phenomenon is called negative bias temperature instability (NBTI). For n-channel MISFET devices, it is called positive bias temperature instability (PBTI).

NBTI was first reported in 1966, for SiO_2/Si based devices [24]. It attracted a lot of interest and was studied in detail [25, 26]. The main mechanisms of NBTI are the creation of interface traps and oxide charge, although it is not well understood when a mechanism dominates over the other [27].

PBTI did not attract so much attention in the past. The reason is that in n-channel transistors, with SiO_2 or SiON dielectrics, PBTI is negligible. However, the introduction of new dielectric materials, mobility enhancers and new three-dimensional device architectures made the PBTI an important reliability issue. Its mechanism is commonly described as filling of preexisting electron traps in the high κ and is thus insensitive to the SiO_2/Si interface [28, 29].

In this thesis, PBTI was assessed for n-channel bulk FinFET with a high κ/TiN gate stack with EOT below 1 nm (Chapter VIII).

PBTI measurement procedure

In this thesis, PBTI is measured by stressing the device, and then interrupting the stress to measure a device parameter (the threshold voltage V_{TH} in this case). The temperature is maintained at 125 °C to simulate operation conditions. The initial V_{TH} and the drain current at $V_G = V_{TH}$ and $V_D = 0.05$ V is determined from an initial I_D-V_G curve. The drain current is measured with minimized delay (a few ms) in order to reduce the recovery effect [30]. This measurement technique is known as measure-stress-measure technique.

During stress, the source, the drain and the substrate are grounded, and a positive voltage V_{stress} is applied to the gate. Between stressing, the gate voltage is switched to V_{sense}, which is chosen equal to the initial V_{TH}, and the drain current is measured at $V_D = 0.05$ V. The threshold voltage shift ΔV_{TH} is then calculated from the difference between the initial I_D and the I_D after stress. Figure III.14a shows the PBTI measurement set-up for a FinFET and figure III.14b shows the voltage pulses that are applied to the gate and the drain during measurements.

If the threshold voltage shift is represented as a function of the stress time t_{stress} for different overdrive voltages (V_{stress} - V_{TH}), as in figure III.15a, it is found that it follows a power law. It can be expressed as:

$$\Delta V_{TH} = C t_{stress}^{\alpha} \qquad \text{equation III.31}$$

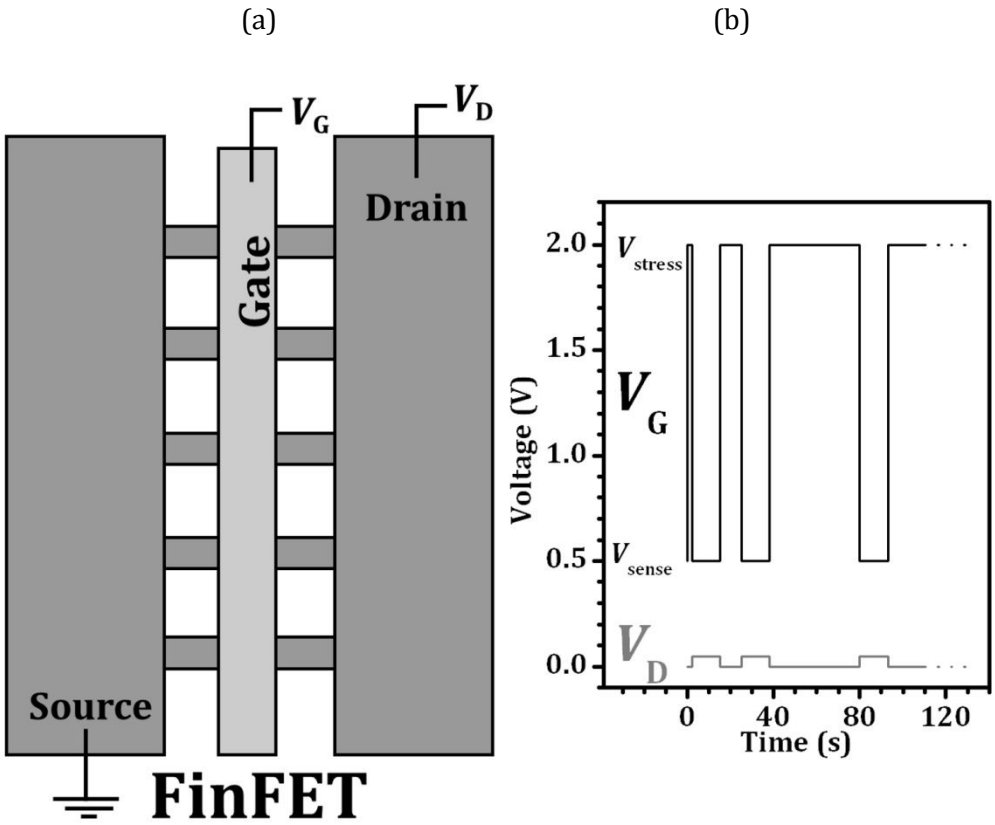


Figure III.14 PBTI measurement set-up.

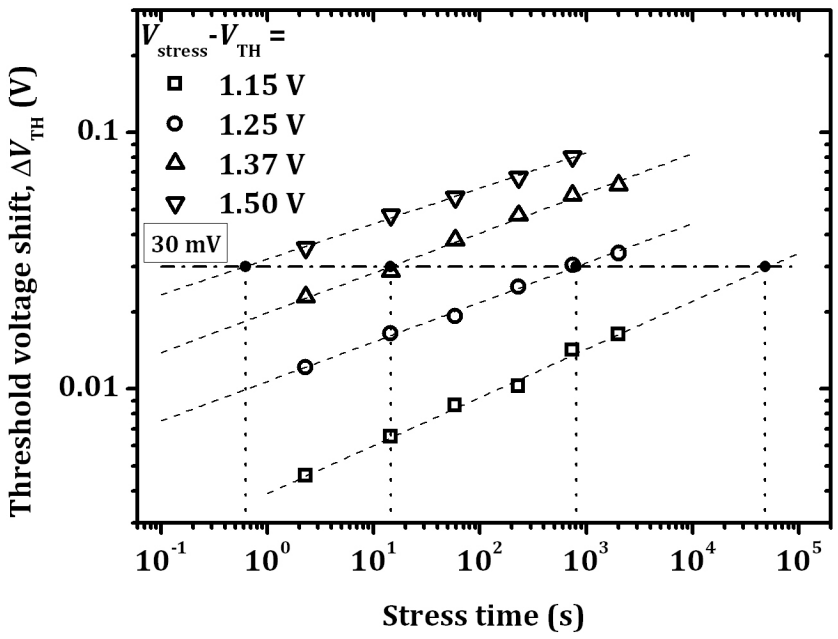
where C and α are constants. The lifetime t_{LF} is thus interpolated or extrapolated using the severe criterion of ΔV_{TH} = 30 mV, as it is shown in figure III.15a. Then, a value of t_{LF} is obtained for each overdrive voltage. The t_{LF} is also assumed to follow a power law with the overdrive voltage (equation III.32).

$$t_{LF} = D(V_{stress} - V_{TH})^{\upsilon} \qquad \text{equation III.32}$$

The parameters D and υ are constants that only depend on the measured device. A common criterion is to extrapolate the overdrive voltage that a transistor can withstand to have a lifetime of 10 years. Figure III.15b illustrates this idea: the t_{LF} is represented as a function of $V_{stress} - V_{TH}$, and the voltage over-drive is obtained for 10 years lifetime.

In order to continue the scaling down of advanced MOSFET devices, overdrive voltage has decreased to 0.6 V [10]. Therefore, the overdrive voltage that a device can withstand for 10 years lifetime at 30 mV of V_{TH} shift criterion is usually extrapolated and compared with the ITRS specifications [10].

(a)



(b)

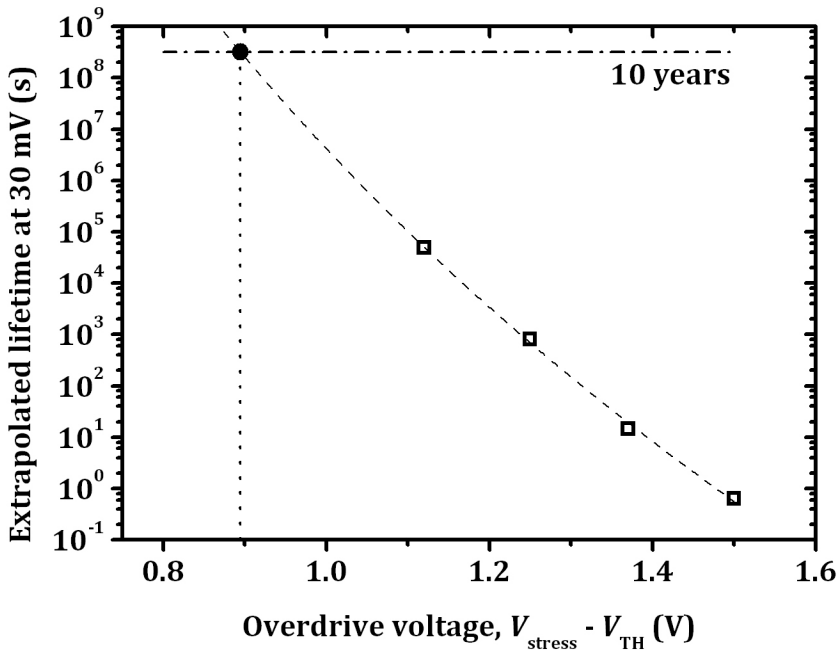


Figure III.15 (a) extrapolation stress time (b) extrapolation overdrive voltage.

III.3 STRUCTURAL CHARACTERIZATION

In this section, the structural characterization techniques used in this thesis are briefly described. Each subsection is dedicated to one technique. It begins with the optical characterization methods: ellipsometry and Fourier transform infrared (FTIR) spectroscopy. It continues with the glancing incidence X-ray diffraction

(GIXRD) and the transmission electron microscopy (TEM). Finally, the compositional analysis methods are discussed: X-ray photoemission spectroscopy (XPS) and time-of-flight secondary ion mass spectroscopy (TOF-SIMS).

III.3.1 ELLIPSOMETRY

Ellipsometry was developed by the German physicist P. Drude in 1888 [31]. It is based on the analysis of the change of polarization of light caused by the reflection on the sample surface. This non-destructive technique obtains the refractive index *n* and the thickness of a transparent thin film t_{ins} deposited on a substrate, if the optical constants of the substrate are known. A schematic figure of this technique is represented in figure III.16.

The electric field of the electromagnetic plane wave can be expressed as the sum of a component parallel to the plane of incidence and a component perpendicular, $\widehat{E_{ip}}$ and $\widehat{E_{is}}$, respectively. The relation between the amplitudes and the phases of both components determine the polarized state of the wave. If $\widehat{E_{ip}}$ and $\widehat{E_{is}}$ are in phase (or 180° out of phase) the polarization is linear. Otherwise, polarization is elliptical. When amplitudes coincide and the components are 90° or 270° out of phase, the polarization is circular.

The components of the reflected wave, $\widehat{E_{rp}}$ and $\widehat{E_{rs}}$, are related to the components of the incident wave through the Fresnel coefficients [32].This coefficients are deduced from the Maxwell equations, applying the corresponding boundary conditions, and they depend

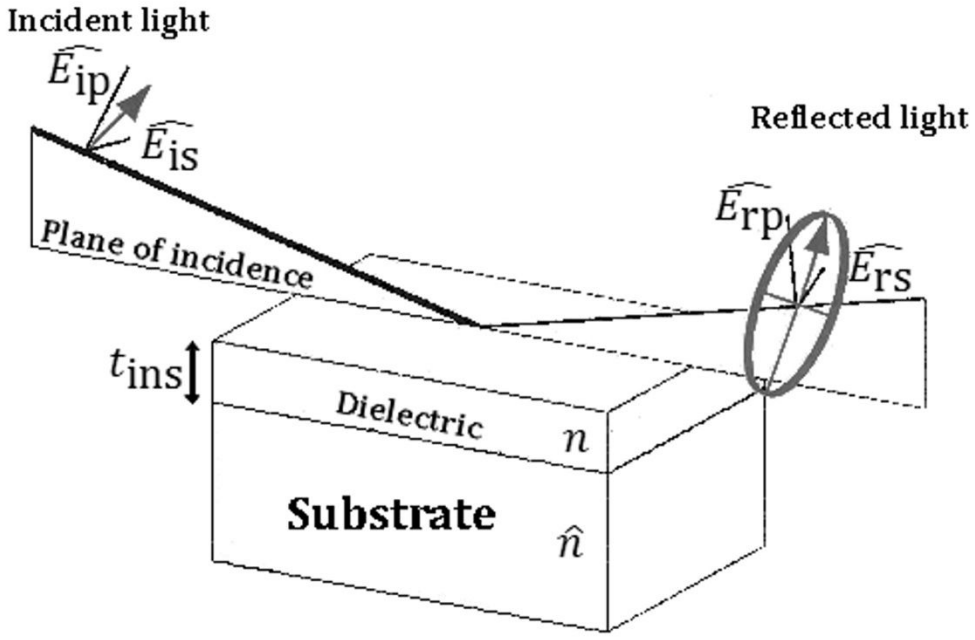


Figure III.16 Schematic figure of ellipsometry.

on the complex refractive index of the substrate $\hat{n}$ and t_{ins}. Equations III.33 and III.34 define Fresnel coefficients.

$$\widehat{E_{rp}} = \widehat{R_p}\widehat{E_{ip}} \quad \text{equation III.33}$$

$$\widehat{E_{rs}} = \widehat{R_s}\widehat{E_{is}} \quad \text{equation III.34}$$

In ellipsometry, two magnitudes are measured, Ψ and Δ, which are defined as in equations III.35, III.36 and III.37.

$$\frac{\widehat{R_p}}{\widehat{R_s}} = \tan(\Psi)\, e^{i\Delta} \quad \text{equation III.35}$$

$$\tan(\Psi) = \frac{|\widehat{R_p}|}{|\widehat{R_s}|} \quad \text{equation III.36}$$

$$\Delta = \arg\left(\widehat{R_p}\right) - \arg\left(\widehat{R_s}\right) \quad \text{equation III.37}$$

Therefore, $\tan(\Psi)$ is the amplitude ratio and Δ is the phase shift difference.

If the sample consists of a transparent film on a reflecting substrate, the reflected wave includes multiple reflections in the film. The refractive index n and the thickness of the film t_{ins} can be determined. The complex refractive index of the substrate $\hat{n}$ must be previously calculated from a measurement of the reflection on the bare substrate.

In this thesis, the thicknesses of ScO_x, GdO_x and $GdScO_x$ films deposited on Si substrates in the range of 4-50 nm were extracted from ellipsometry. It was measured with a *Nanofilm EP³* ellipsometer, which is provided with a 532 nm laser. The incidence angle was 70°. The measurements were performed in the "*CAI de Espectroscopía*" of the Complutense University of Madrid.

III.3.2 Fourier transform infrared (FTIR) spectroscopy

Fourier transform infrared (FTIR) spectroscopy is a non-destructive technique that studies the interaction of materials with infrared radiation. Infrared light is absorbed by chemical bonds and converted into vibration energy. When the radiant energy matches the energy of a specific vibration mode, absorption occurs.

The Fourier transform infrared spectrometer is based on the Michelson interferometer [33]. The schematic of the spectrometer is depicted in figure III.17. An infrared light source emits a beam that is split by a mirror that reflects 50% of the light and transmits the remaining 50% (the beam splitter). The reflected beam is reflected again in a fixed mirror while the transmitted one is reflected by a moving mirror that introduces a path length difference *2x*. Both beams are merged again by the beam splitter. For a monochromatic light source, with angular

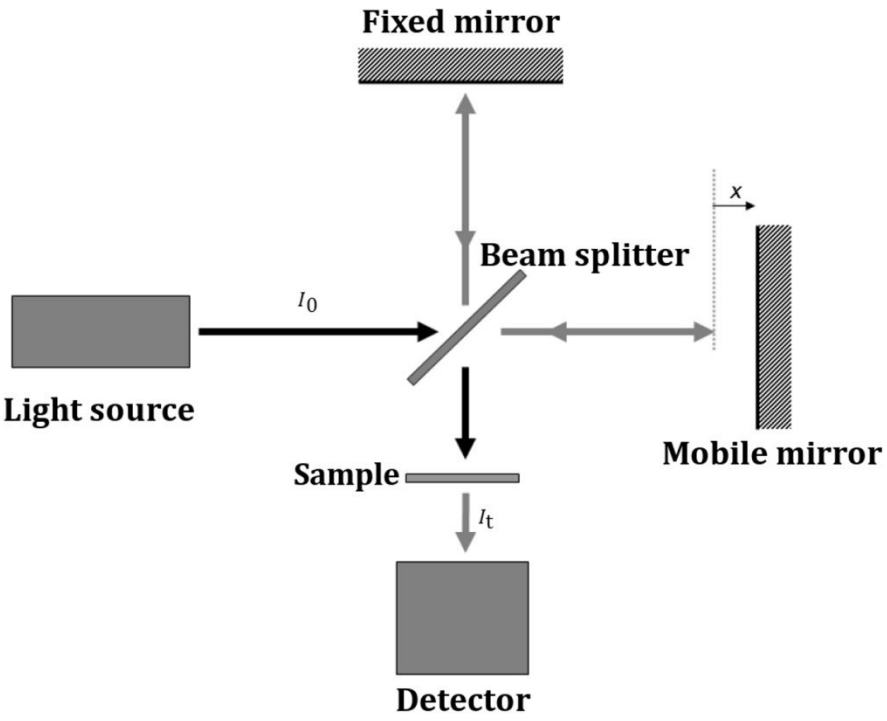


Figure III.17 Schematic image of a Fourier Transform spectrometer.

frequency ω and intensity $2I_0$, the intensity of the resultant beam I would follow equation III.38.

$$I = I_0\left(1 + \cos\left(\frac{\omega}{c}2x\right)\right) \qquad \text{equation III.38}$$

Thus the intensity transmitted through the sample would follow equation III.39.

$$I_t = T(\omega)I = T(\omega)I_0\left(1 + \cos\left(\frac{\omega}{c}2x\right)\right) \qquad \text{equation III.39}$$

where $T(\omega)$ is the transmittance of the sample. However, the source emits light with wavelength-independent intensity $2I_0$. Then, the detector measures the following intensity $I(x)$ as a function of the mirror position x:

$$I(x) = I_0\int_0^\infty T(\omega)d\omega + I_0\int_0^\infty T(\omega)\cos\left(\frac{\omega}{c}2x\right)d\omega \qquad \text{equation III.40}$$

The first term is a constant while the second one represents the Fourier transform of the transmission $T(\omega)$. Then, $I(x)$ can be measured by the detector and the inverse Fourier transform gives $T(\omega)$. In FTIR spectra, the absorbance A, as defined in equation III.41, is usually represented in the ordinate. In the abscissa, the wavenumber $\bar{\nu}$ is used, which is the inverse of the wavelength λ and is expressed in cm^{-1} (equation III.42).

$$A(\omega) = \log_{10}\frac{1}{T(\omega)} \qquad \text{equation III.41}$$

$$\bar{\nu} = \frac{1}{\lambda}$$ equation III.42

Then, the wavenumber is proportional to the photon energy E:

$$E = hc\bar{\nu}$$ equation III.43

where h is the Planck constant and c is the speed of light.

This technique is used through this thesis to analyze the bonding structure of the growing film and the high κ/semiconductor interface.

The substrates used for FTIR measurements are 2-inch 200 or 300 µm thick n-Si (100) wafers polished on both sides, with high resistivity (200-1500 Ω cm) doped with phosphorus. The absorbance spectra of the samples include the substrate absorption. Thus this contribution must be corrected by subtracting the spectrum of bare silicon, which is obtained before each measurement.

The spectra of samples give information on the interface layer through the asymmetric stretching vibration mode of SiO_2 [34]. In chapter IV, the SiN_x is studied as an alternative to SiO_2 for interfacial layer. The stretching vibration mode of Si_3N_4 [35] helps in the analysis of the electrical results of the samples. FTIR in the mid infrared also confirms the presence of Sc-O and Gd-O bonds in dielectric films [36].

The FTIR spectra were taken in the 400-4000 cm^{-1} range by a *Nicolet Magna-IR 750 series II* spectrometer. An *ever-Glo* source was used and the detector was provided with a deuterated triglycine sulfate window of KBr. Obtained spectra have a resolution of 16 cm^{-1}. Measurements were performed in the "*CAI de Espectroscopía*" of the Complutense University of Madrid.

III.3.3 Glancing incidence X-ray diffraction (GIXRD)

X-ray diffraction (XRD) is a powerful technique for the investigation of the crystal structure of solids. Its origin dates back to the beginning of the 20th century, when the German physicist von Laue discovered that crystalline solids produced surprising patterns of diffracted X-rays. In 1913, W.H. Bragg and W.L. Bragg gave a physical explanation for the diffraction patterns [37].

When X-rays reach a crystalline solid, the atoms scatter them in all directions. Electron clouds of atoms respond to the electric field of the X-ray, oscillating with the same frequency. These accelerated charges spread out their own

electromagnetic field in all directions, identical in wavelength and phase to the incident X-ray. In some of these directions the scattered beams are completely in phase and so they interfere to form diffracted beams. The directions of the diffracted beams are determined by the arrangement of the atoms in the solid. Thus, the diffraction pattern gives information on the crystal structure.

The Bragg law predicts the diffraction direction θ_{hkl} from the distance between crystallographic planes d_{hkl}, and the X-ray wavelength λ [38]. The *hkl* subscripts are called Miller indices and denote the planes considered in the diffraction. The Bragg law is obtained by imposing that the difference of the optical path $2d \sin(\theta_{hkl})$ by different scattered X-rays is n times the wavelength λ, with n being an integer.

$$2d_{hkl} \sin \theta_{hkl} = n\lambda \qquad \text{equation III.44}$$

The Bragg law gives the direction of the diffracted beams, but it does not provide any information on their intensity. This intensity of the diffracted beam depends on the square of the structure factor F_{hkl}. This parameter is determined solely by the atoms and their arrangement in the unit cell of the crystal. It is important to note that this factor can be zero, giving the so-called forbidden reflections or extinctions. This means that there are reflections predicted by the Bragg law that do not appear in the XRD pattern.

In this thesis, the X-ray diffraction patterns were obtained by glancing incidence XRD (GIXRD) configuration. Glancing angle diffraction techniques are used when the information needed lies within a thin top layer of the material [39]. In GIXRD, the beam comes in contact with the surface of the sample at a fixed small angle ω (<0.5°), while the detector makes a 2θ scan [40]. A schematic view of this configuration can be seen in figure III.18. The result of the glancing incidence angle is an increase of the path traveled by the X-ray signal through the thin layer and a reduction of the diffraction of the substrate. The irradiated region of the sample also increases from 0.5 mm in the conventional θ-2θ configuration up to ~35 mm at glancing angle. Conventional XRD gives information on a top layer of a thickness in the order of micrometers. In contrast, by employing a glancing angle technique this thickness may be three orders of magnitude smaller, allowing studying films with a thickness of few nanometers.

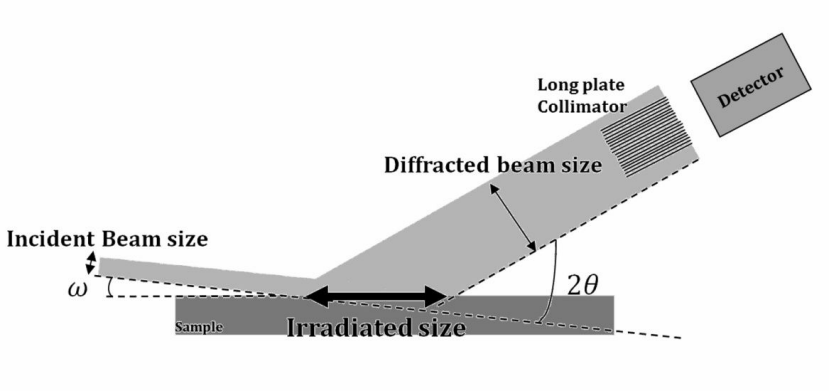


Figure III.18 Schematic image of GIXRD.

GIXRD patterns were used along this thesis to identify Gd_2O_3 and Sc_2O_3 crystal phases in thin layers. For Sc_2O_3, the cubic bixbyte phase is the only known polymorph [41]. In the case of Gd_2O_3, it can present the monoclinic or the cubic phase [42, 43].

The diffraction patterns were obtained at the "*CAI de difracción de rayos X*" of the Complutense University of Madrid using a *Panalytical X'Pert PRO MRD*. The wavelength of the X-ray beam was λ = 0.1541 nm corresponding to the Cu K_α line.

III.3.4 TRANSMISSION ELECTRON MICROSCOPY (TEM)

The Transmission Electron Microscopy (TEM) is based on the interaction between an electron beam and the atoms of a sample. The beam is focalized and accelerated towards the sample, which must be thin enough to allow part of the electrons to be transmitted. The resultant beam forms an image on a screen or on an image recording system.

The main advantage of this technique is obtaining images of the sample in the nanometer scale, while optical microscopy is limited to the scale of microns. This is due to the fact that the resolution is given by the wavelength of the light used by the microscope. Wavelength of visible light is in the 400-700 nm range while the electron wavelength in the Ångstrom range. The first TEM microscope with higher resolution than optical microscopes was built by the German physicists Knoll and Ruska in 1933 [44].

The main components of a TEM microscope are the electron source, the electromagnetic lenses and the detector (a fluorescent screen, a digital camera or a

photographic film). Figure III.19 depicts a schematic diagram of a TEM microscope. The condenser electromagnetic lens guarantees a parallel electron beam through the sample. The electrons can either cross unaffected or be scattered by the atoms of the sample. Transmitted electrons form an image that is focused by the lens system on the detector.

TEM microscopy was used along this thesis to analyze the dielectric films deposited on Si and the gate stacks of MIS capacitors. The thickness, the roughness, the crystallinity and the possible growth of an interfacial layer can be studied from the image of the stacks.

Additionally, TEM microscopes are often provided with a measurement system of energy dispersive X-ray (EDX) spectrometry. It allows chemical analysis of the samples, since it analyzes the X-rays emitted as a result of the interaction between the sample and the electrons of the beam.

The TEM characterization was carried out in the "*CAI de Microscopíaelectrónica*" of the Complutense University of Madrid. One of the TEM microscopes used in this thesis is a *JEOL JEM-2000FX* at 200 keV. In selected samples, high resolution TEM was performed with a *JEOL JEM-4000EX* at 400 keV. TEM images were also taken with a *Tecnai T20* microscope from *FEI*, at 200 keV, in the "*Instituto de Nanociencia de Aragón*". These microscopes are provided with an EDX spectrometer for chemical characterization of the samples.

Sample preparation

The sample preparation is the main drawback of the TEM technique. Cross section samples require careful, time-consuming and expensive preparation to produce samples thin enough to be electron transparent (~100 nm). Cross sectional TEM samples were prepared according to the following procedure:

1. formation of a stack with two slices of the samples so that the thin films face each other;
2. mechanical polishing of the stack, up to a thickness of 100 μm;
3. one-side sphere-shaped deepening using a dimple-grinder;
4. Ar ion milling until a hole is opened.

The last step is the most harmful in TEM cross-sectional sample preparation. However, for silicon based samples, the parameters of this process are optimized, so the damage is very low. All the equipment was provided by the "*CAI de Microscopía*" of the Complutense University of Madrid. Cross sectional samples were also prepared in the "*Instituto de Nanociencia de Aragón*".

Additionally, TEM samples were prepared by the H-bar focused ion beam (FIB) technique [45] in the "*Plataforma de Nanotecnología*" of the "*Parc Cientific de*

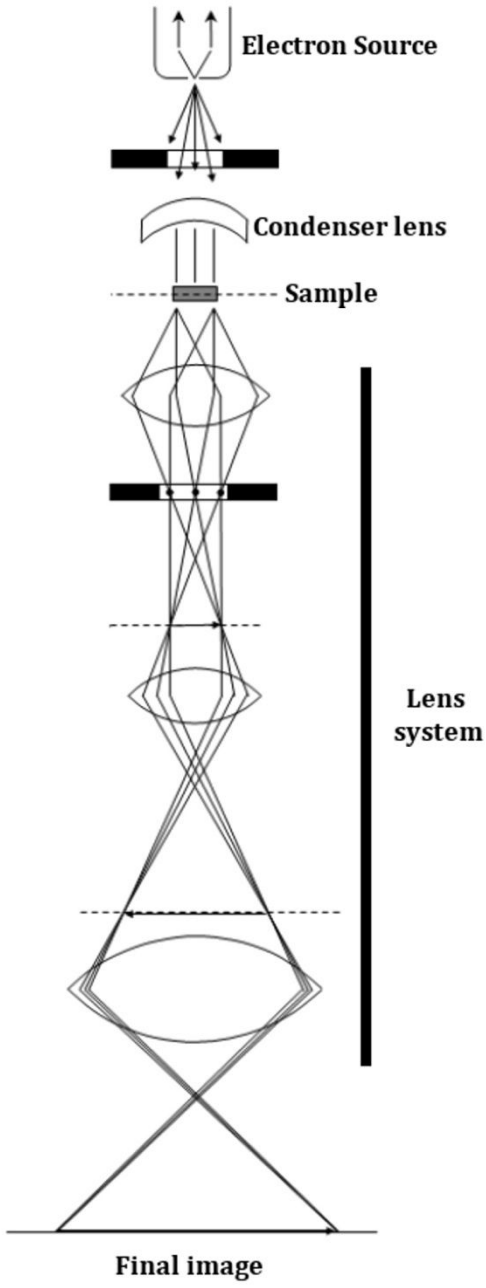


Figure III.19 Schematic image of TEM imaging in the direct operation mode.

Barcelona." This technique requires a pre-thinning of the sample (up to 70 μm). Then, an Ar ion beam cut two deep trenches that leave a lamella that is able to be analyzed in the TEM microscope.

Lastly, samples were prepared by the *ex-situ* lift out technique [45]. In this method, a specific region is FIB milled to electron transparency, and then the thin lamella is removed from its trench with a micromanipulator. This preparation was performed in the "*Instituto de Nanociencia de Aragón*".

III.3.5 X-RAY PHOTOEMISSION SPECTROSCOPY (XPS)

X-ray photoelectron spectroscopy (XPS) is a non-destructive technique that is based on the photoelectric effect discovered by Hertz in 1887 and explained by Einstein in 1905. This technique was developed by the Swedish physicist Siegbahn in the 1960s [46, 47]. It is mainly used for identifying chemical species at the sample surface.

An schematic view of XPS operation is observed in figure III.20. The X-ray photons excite core level electrons, which are emitted from their state with an energy that exceeds the binding energy (BE). The kinetic energy of the ejected electrons E_K is measured at a spectrometer. Then, if the incident X-ray photon has an energy $h\nu$, the BE, E_b, of the electron in the core level can be calculated according to equation III.45.

$$E_b = h\nu - E_K \qquad \text{equation III.45}$$

The incident X-ray energy must be monochromatic, in order to know accurately the energy of the incident photons. XPS spectra represent the number of electrons that are excited with certain BE.

The electron BE is a distinguishing characteristic of each element. Also, it is influenced by its chemical surroundings, so the BE determines the chemical state of the atom. Tables and databases are available for element and chemical identification [48].

Although the incident X-rays penetrate deep in the sample, the detected electrons are ejected from the ~3 nm thick upper part of the sample. The electrons excited within the sample are absorbed by other atoms inside the sample and cannot reach the detector. Thus the analysis is limited to the sample surface.

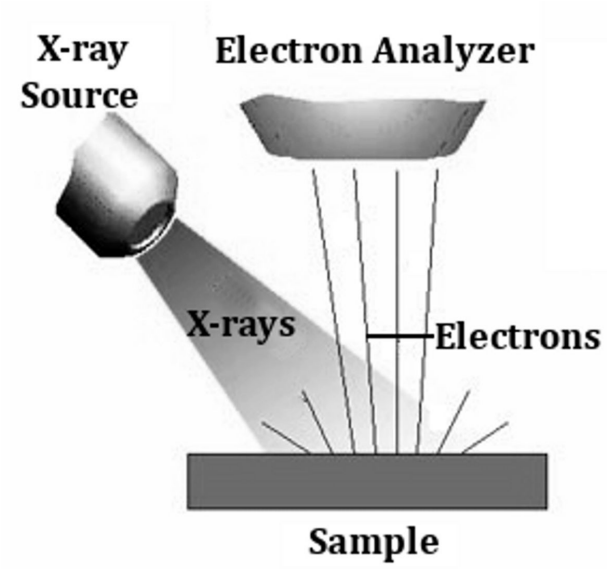


Figure III.20 Schematic image of XPS.

Peak areas can be used with appropriate correction factors to obtain densities [48, 49]. In this thesis, XPS was used to calculate the atomic ratios of the components in the samples. This way, the stoichiometry of the $Gd_{2-x}Sc_xO_3$ and the oxides Sc_2O_3 and Gd_2O_3 was assessed, assuming a constant composition in the whole film.

XPS spectra were obtained with a *VG Escalab 200R* spectrometer equipped with a Mg K_α X-ray source ($h\nu$ = 1254.6 eV), powered at 120 W. The background pressure in the analysis chamber was maintained below 2×10^{-8} mbar during data acquisition. The XPS data signals were taken in increments of 0.1 eV with dwell times of 50 ms. Binding energies were calibrated relative to the C 1s peak at 284.9 eV. Measurements were performed in the "*Instituto de Catálisis y Petroleoquímica*" of the "*Consejo Superior de InvestigacionesCientíficas*."

III.3.6 TIME-OF-FLIGHT SECONDARY ION MASS SPECTROSCOPY (TOF-SIMS)

The Time of flight secondary ion mass spectroscopy (TOF-SIMS) allows compositional analysis of sample surface. The SIMS fundamentals were developed by Herzog and Viehboeckin 1949. In 1958, Honig built the first complete secondary-ion mass spectrometer with sputter depth profiling. In the 1970s, Benninghoven, Niehus and Steffens introduced the TOF mass spectrometers to the SIMS at the University of Münster, Germany [50].

This technique gives the depth profile of element concentrations with high sensibility [51]. It is a destructive technique and consists in bombarding the sample with a pulsed high energy Bi ion beam, which desorbs and ionizes atoms or molecules from the sample surface. An schematic representation of the TOF-SIMS operation can be seen in figure III.21. The emitted ions, called secondary ions, are accelerated towards a TOF mass spectrometer. The mass spectrometer selects the ion mass through the energy of the particle. Finally, ions are directed to the detector, where they are quantified. A second Cs or Ga ion beam sputters the surface during measurement, creating a hole, in order to get the depth profile of the detected species.

TOF-SIMS allows the identification of ionized molecules and all elements. However, the concentration profile is relative, since each species has a different ionization probability. Then, for stoichiometry assessment, some other technique must be used, such as XPS, explained in section III.3.5.

In this thesis, TOF-SIMS was used to analyze the composition of the thin dielectric films deposited on Si and the dielectric/Si interface. In chapter IV, this technique is especially useful in the study of the $ScO_x/SiO_x/Si$ and $ScO_x/SiN_x/Si$ interfaces.

The mass spectra of the samples were recorded on a *TOF-SIMS IV* instrument

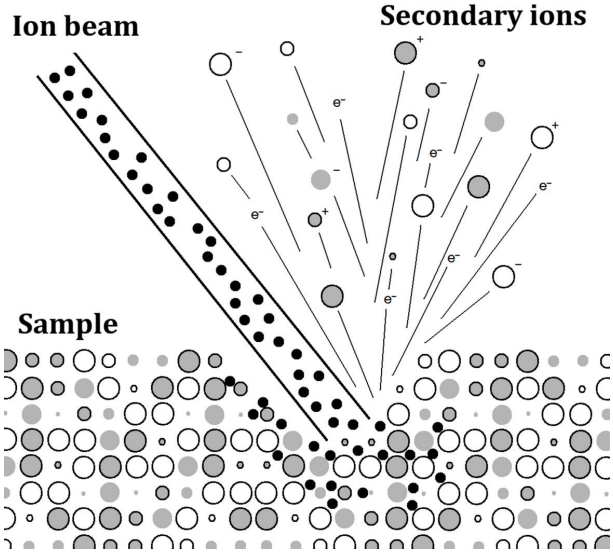


Figure III.21 Schematic image of TOF-SIMS operation.

from *Ion-Tof GmbH Germany*. The sample was bombarded with a pulsed Bi ion beam. The secondary ions generated were extracted with a 10 kV voltage and their time of flight from the sample to the detector was measured in a reflection mass spectrometer. Typical analysis conditions were:

- 25 keV pulsed Bi beam at 45° incidence, rastered over 250×250 μm^2, for mass spectrometry;
- Cs gun at 2 keV, rastered over 350×350 μm^2, for sample sputtering and depth profile.

The TOF-SIMS measurements were performed by the "*Servicio de Nanotecnología y Análisis de Superficies*" of the "*Centro de Apoyo Científico a la Investigación*" (CACTI) of the University of Vigo.

III.4 SUMMARY

This chapter stated the fundamentals of the MIS capacitors that were analyzed through this thesis. All the electrical, structural and reliability characterization techniques used in this thesis were listed, with a brief background to understand each technique and a specification of the measurement conditions. Throughout this chapter, the importance of the experimental measurements in this thesis was highlighted.

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CHAPTER IV. SCANDIUM OXIDE/SILICON INTERFACE CHARACTERIZATION

As it was stated in chapter I, a vital issue of high κ dielectrics is their interface with Si [1, 2]. An interface with a high roughness or a high density of defects scatters the carriers in the transistor channel, degrading their mobility [3]. The defects in the interface also cause unreliability, since trapped charge is the starting point of a failure and consequent breakdown of the dielectric. Moreover, charge can be trapped in the defects of the interface during stress operation, affecting the threshold voltage of the device (the voltage at which it turns on) [4]. These problems that the high κ dielectrics show were partially solved with the use of an extremely thin (1 nm or below) SiO_2, thermally or chemically grown on the Si surface prior to the high κ dielectric deposition [5, 6]. Such approach proved to be reasonably effective to solve some problems, but different alternatives should be also explored since it imposes an equivalent oxide thickness (EOT) limit.

Among the possible alternatives to further reduce interfacial SiO_2 thickness, the use of silicon nitride (SiN_x) as an interfacial layer between high κ and silicon to decrease the EOT of the structure is proposed in this thesis [7]. In fact, the relative dielectric constant of Si_3N_4 ($\kappa_{SiN} \sim 8$) is about twice that of SiO_2. For poly-Si/high κ stacks, EOT scaling using SiN_x interlayers was demonstrated [8, 9]. However, this interfacial layer also proved to reduce the carrier mobility in the transistor channel, probably caused by scattering of trapped positive charges generated by N in the interface [8]. Although this seems a major drawback, the question whether the effect of SiN_x on carrier mobility is less severe than the SiO_2 reduction remains unsolved [7].

In this chapter we study the physical and electrical properties of a high κ/Si interface. The selected high κ is scandium oxide grown by high pressure sputtering (HPS). The Si substrates were differently prepared in other to provide several surfaces where the Sc_2O_3 could be deposited onto. The samples were physically characterized by Fourier transform infrared spectroscopy (FTIR), glancing-incidence X-ray diffraction (GIXRD), time-of-flight secondary ion mass

spectroscopy (TOF-SIMS), X-ray photoemission spectroscopy (XPS), and transmission electron microscopy (TEM). Al gated metal-insulator-semiconductor (MIS) devices were fabricated for the electrical characterization of the samples. The substrates used for comparison were: bare-Si, chemical SiO_2 and several types of SiN_x (deposited and nitrided Si surface). This way, we compare different interfaces: native SiO_2, SiO_2 regrown from the sputtering and SiN_x with several preparations.

IV.1 Experiment

The stacked structures were fabricated on single side polished n-Si (100) wafers with a resistivity of 1.5-5.0 Ω cm. To measure the infrared absorbance of the different stacks, double side polished n-Si (100) wafers with a resistivity of 200 - 1000 Ω cm were used. All wafers were cleaned using a standard RCA (*Radio Corporation of America*) process.

Scandium oxide was deposited on five differently prepared Si substrates: (1) H-terminated Si surface, (2) RCA native oxide, (3) SiN_x deposited and (4-5) nitrided Si for different times. The H-terminated Si surface was achieved by an etching process of the RCA cleaned substrates in a HF diluted solution for 30 s. This was performed immediately before the introduction of the sample to the HPS chamber. SiN_x was deposited with an electron-cyclotron-resonance chemical vapor deposition system (ECR-CVD) [10] using high purity N_2 and SiH_4 as precursor gases, with a N_2/SiH_4 ratio of 9:1 and a total gas flow of 10.5 sccm. The base pressure was 7×10^{-7} mbar. The processing gases yielded a constant pressure of 9×10^{-4} mbar during deposition. The microwave power was fixed at 100 W and the deposition temperature at 200 °C. Finally, ECR nitridation was carried out using N_2 at a 10.5 sccm flow for 30 s and 10 min (with the same conditions as the SiN_x deposition, 100 W and 9×10^{-4} mbar). ECR samples were HF-etched in N_2 atmosphere just before deposition and transferred to the ECR chamber without being exposed to atmosphere.

The scandium oxide films were deposited on the differently processed substrates by HPS in pure Ar atmosphere. The deposition conditions for all samples were identical; hence the only intentional difference was the starting substrate. The deposition pressure was 0.50 mbar (base pressure 2×10^{-6} mbar). A

commercial 4.5 cm diameter high purity Sc_2O_3 target was used. The 13.54 MHz radio frequency (*rf*) power was kept at 40 W. Depositions were performed for 2 h keeping the substrate temperature at 200 °C.

For electrical characterization, 500 × 500 μm^2 metal-insulator-semiconductor (MIS) devices were defined by e-beam evaporation of Al electrodes followed by standard lithography process. After top electrode definition, Al was evaporated to the backside and the samples were annealed for 20 min at 300 °C in forming gas atmosphere (FGA process).

The infrared absorbance of the samples was measured by FTIR in the 400-4000 cm^{-1} range in transmission mode at normal incidence to study the chemical bonds of the grown layers. The spectra were substrate corrected. The substrate used for correction is a RCA cleaned wafer, which is thus covered by a chemical oxide. GIXRD was measured at $\omega = 0.5°$ in order to study crystal structure of deposited scandium oxide films. TEM measurements determine the thickness and morphology of the films. XPS of the samples was obtained with a Mg K_α ($h\nu$ = 1254.6 eV) X-ray source. Binding energies were calibrated relative to the C 1s peak at 284.9 eV. Symmetric Gaussian-Lorentzian functions (90G/10L) were used to approximate the line shapes of the fitting components. Atomic ratios were computed from experimental intensity ratios and normalized by atomic sensitivity factors [11]. For TOF-SIMS analysis, mass spectra were recorded on the samples sputtered with an O_2 gun at 2 kV (rastered over 500×500 μm^2) and bombarded with a 25 keV pulsed Bi^{3+} beam at 45° incidence (rastered over 250×250 μm^2) for analysis. Generated secondary ions were extracted with a 10 kV voltage and their time of flight from the sample to the detector was quantified in a reflectron mass spectrometer.

MIS devices were electrically characterized by the high-frequency/quasi-static (C_{HF}- and C_{QS}-V_G) method [12]. From these measurements, we calculated the EOTs of the stacks. The energy distribution of interface traps (D_{it}) can be calculated as long as the gate leakage is low enough to avoid quasi-static capacitance distortion. For comparison, G-V_G measurements were performed to evaluate D_{it} by the conductance method [12]. Finally, the gate leakage current of the stacks was obtained at inversion as a function of gate bias voltage.

IV.2 RESULTS AND DISCUSSION

IV.2.1 STRUCTURAL CHARACTERIZATION

Figure IV.1a shows representative FTIR spectra of the stacks in the 400-1200 cm^{-1} range. Outside this region spectra present no other significant features. The peak at 667 cm^{-1} is characteristic of the C-O bond [13] and it is caused by the presence of CO_2 in the chamber of the measurement system, so it will not be further discussed. Two main features appear clearly in the FTIR spectra: between 400-500 cm^{-1} in all samples and between 800-1100 cm^{-1} only in nitrided samples.

Firstly we discuss the 800-1100 cm^{-1} region. Figure IV.1b shows this region in large detail. The nitrided samples present a wide and quite flat band centered around 900 cm^{-1} and a valley-like feature around 1065 cm^{-1}. Due to the flatness of the peak together with the baseline of the spectra it is difficult to assure where the maximum is located. Stoichiometric Si_3N_4 has a stretching vibration mode [14] at 835 cm^{-1} so the measured band can be attributed to the formation of SiN_x during the nitridation process. The shift towards higher wave numbers may be related to O incorporation to this passivation layer as a contamination from the ECR quartz chamber [15]. Also, the width of the band points to a quite disordered layer. In other words, the angle and distance value spread of the Si-N bonds is bigger than relaxed Si_3N_4 films, and this distribution gives rise to a wider distribution of resonance frequencies. This band is slightly more apparent for the longer nitridation time, which means a thicker SiN_x layer.

The valley at 1065 cm^{-1} is caused by the substrate signal correction as the bare substrates used for correction have a 1-2 nm thick chemical oxide due to the RCA process [16]. This indicates that the content of Si-O bonds in the nitrided samples is lower than in the reference substrate, i. e., the thickness of the interfacial SiO_x in the nitrided samples (if present) is lower than in the RCA chemical oxide. The un-nitrided samples do not show any peak or valley at 1065 cm^{-1}, which indicates that the SiO_x thickness in the stack must be comparable to the RCA chemical oxide.

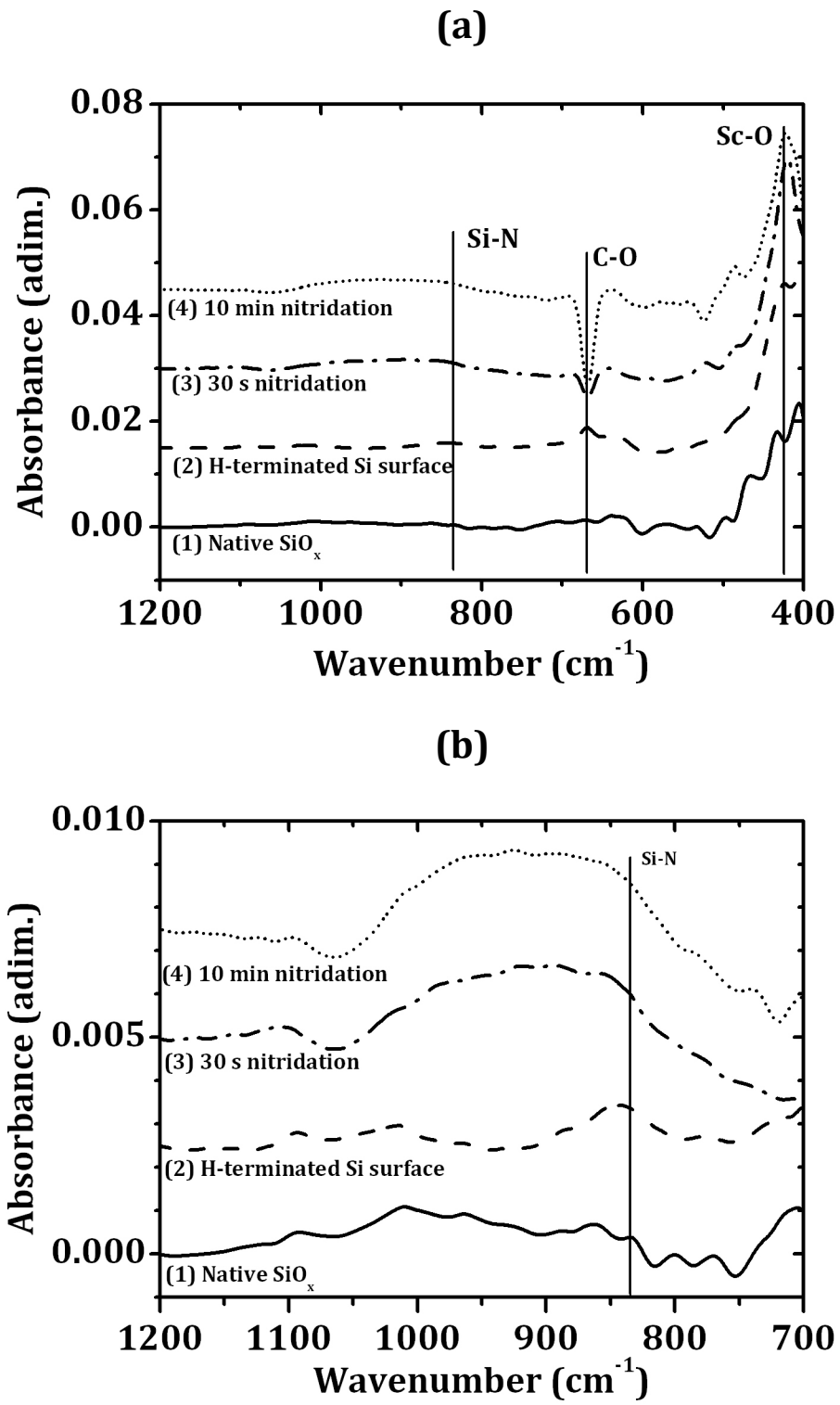

Figure IV.1 (a) FTIR spectra of the stacks in the 1200 - 400 cm^{-1} region: (1) scandium oxide deposition on RCA chemical SiO_x, (2) deposition after etching in HF dilute solution, (3) after 30 s nitridation, and (4) after 10 min nitridation. (b) Zoom in the 1200-700 cm^{-1} region.

To gain further insight into the nitride passivation role, FTIR spectra of SiN_x layers were also obtained before Sc_2O_3 sputtering deposition and they are represented in figure IV.2a. Comparing the spectra before and after sputtering of Sc_2O_3 for both nitridation times in figure IV.2b, we observe that the band at 900 cm^{-1} and the valley at 1070 cm^{-1} remain after deposition. Thus, the SiN_x layer is still present and there is no detectable SiO_x regrowth during sputtering. Analogous results were extracted for deposited SiN_x in previous works [17].

The increase in the absorbance in the 400-500 cm^{-1} range can be associated to Sc-O bonds. This is confirmed by FTIR spectra before and after Sc_2O_3 deposition in figure IV.2a. Before sputtering, the region between 400 and 500 cm^{-1} remains almost flat, but after scandium oxide deposition a peak appears with its maximum at about 420 cm^{-1}. Hardy *et al.* found FTIR peaks at 609 and 711 cm^{-1} for Sc_2O_3 deposited layers [18]. Also, other works proposed Sc_2O_3 FTIR absorption peaks at 625 and 425 cm^{-1} [19]. The samples in this experiment do not present any peak at 609 or 711 cm^{-1} and at 625 cm^{-1} it is difficult to assure it since it is very close to the CO_2 absorption. However, all samples with the ScO_x layer, including un-nitrided samples from figure IV.1, present the increase in the absorbance in the region around 425 cm^{-1}, which supports the conclusion of being related to Sc-O bonds.

Concerning the crystal structure of the stacks, figure IV.3 shows the GIXRD patterns of the deposited scandium oxide films. The only known polymorph of Sc_2O_3 is the cubic bixbyite phase [20]. The most intense peaks of this Sc_2O_3 cubic phase are marked in the graphic. The patterns show that all samples, independent on the substrate type, crystallize in the same cubic phase, without relevant differences. In most samples it can be appreciated that there is a remaining of the (113) plane of the crystalline Si substrate at 2θ = 56.4°. This is caused by the relatively low thickness of the scandium oxide film and the glancing incidence of the X-rays. According to the relative intensity of the Sc_2O_3 peaks, there is no preferential direction in the poly-crystalline growth.

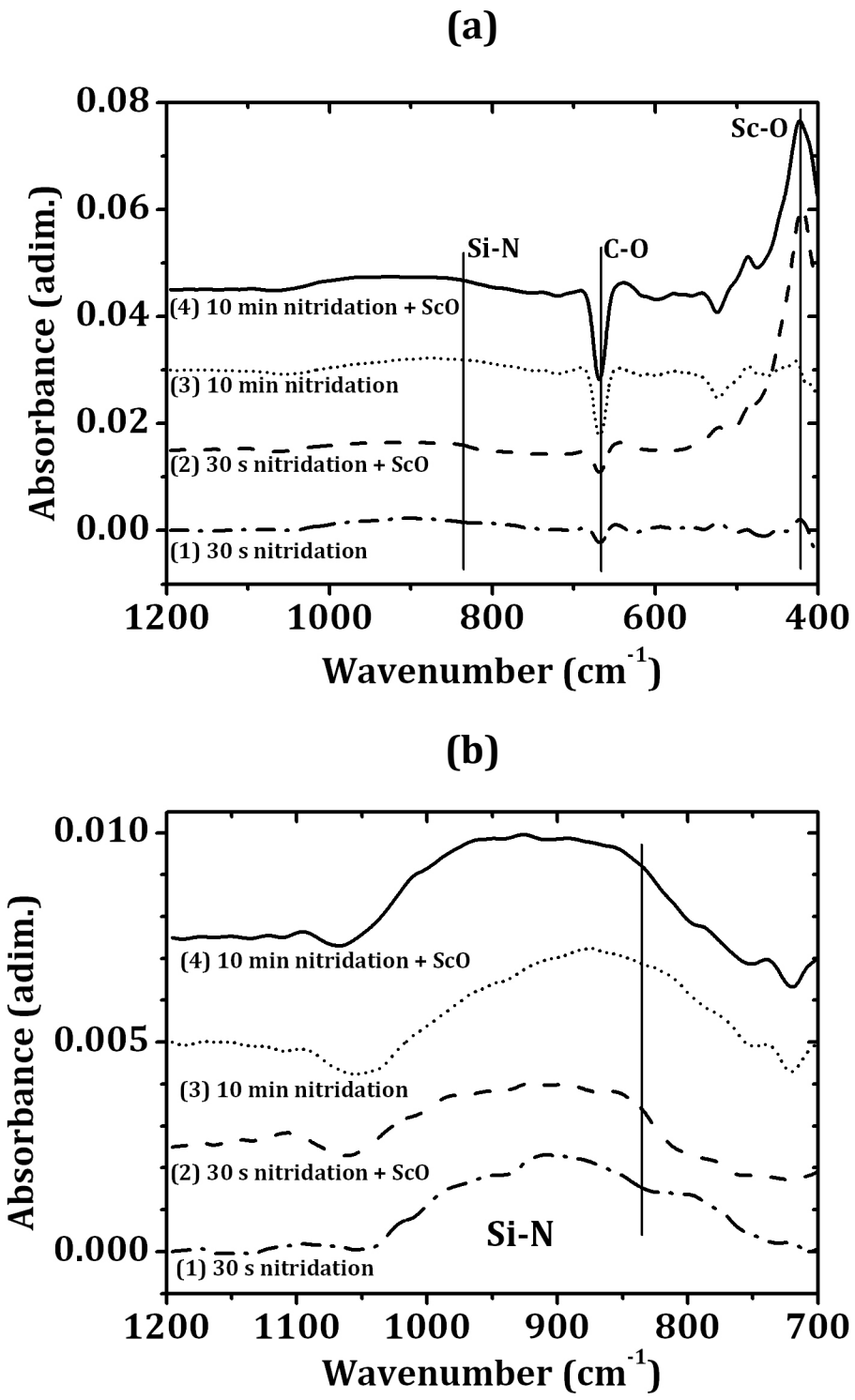

Figure IV.2 (a) FTIR spectra of the silicon nitride layers in in the 1200 - 400 cm^{-1} region: (1) 30 s nitridation, (3) 10 min nitridation, (2) 30 s nitridation + Sc_2O_3 deposition, and (4) 10 min nitridation + Sc_2O_3 deposition. (b) Zoom in the 1200 - 700 cm^{-1} region.

We then conclude that the as-deposited films are poly-crystalline, and they do not need further heat treatments to crystallize. It must be noticed that the highest temperature that these Sc_2O_3 films reached is 200 °C during deposition

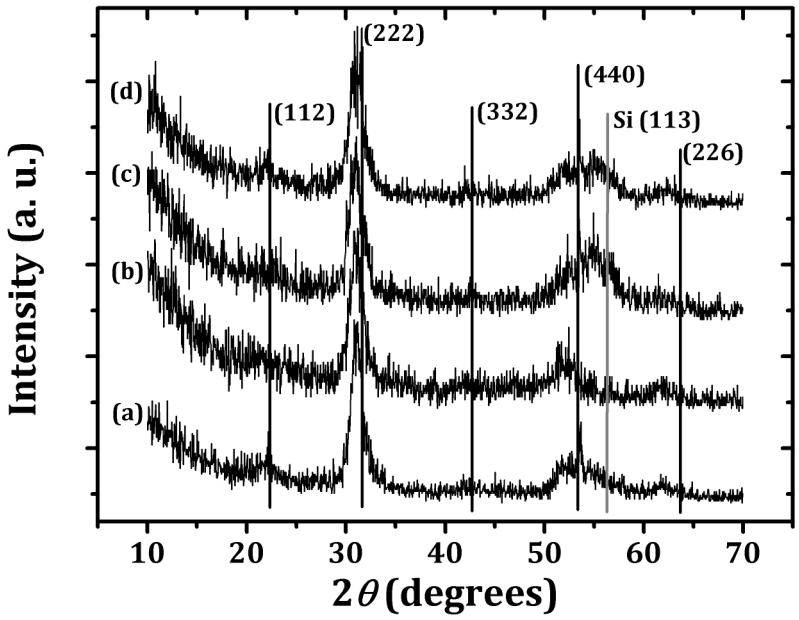

Figure IV.3 GIXRD diagrams of Sc_2O_3 films deposited on (a) RCA chemical oxide, (b) H-terminated Si surface, (c) 10 min nitrided Si surface, and (d) 30 s nitrided Si surface. The marked crystallographic planes correspond to the most intense peaks in Sc_2O_3 cubic phase.

process. This is an advantage for memories, where crystal phases are preferred due to their higher dielectric permittivity, but the crystallization temperature should remain below 650 °C in order to enable successful integration with device fabrication [21]. Also, the starting substrate does not seem to affect the growth behavior of the high κ film.

Figure IV.4 shows TOF-SIMS profiles of the samples where Sc_2O_3 was deposited on (a) H-terminated Si and (b) 10 min ECR nitrided Si. In the first sputtering cycles the amount of detected ScO is constant with depth for all samples. When the scandium oxide film ends, an increase on the SiO signal can be observed, and also on SiN in the case of nitrided and SiN_x deposited samples. Finally, after the interface end, the Si counts rise to a constant level, indicating that the measurement reached the substrate. Thus, the conclusion is that a Sc_2O_3 film with a constant composition with depth is grown, with no contamination from the substrate.

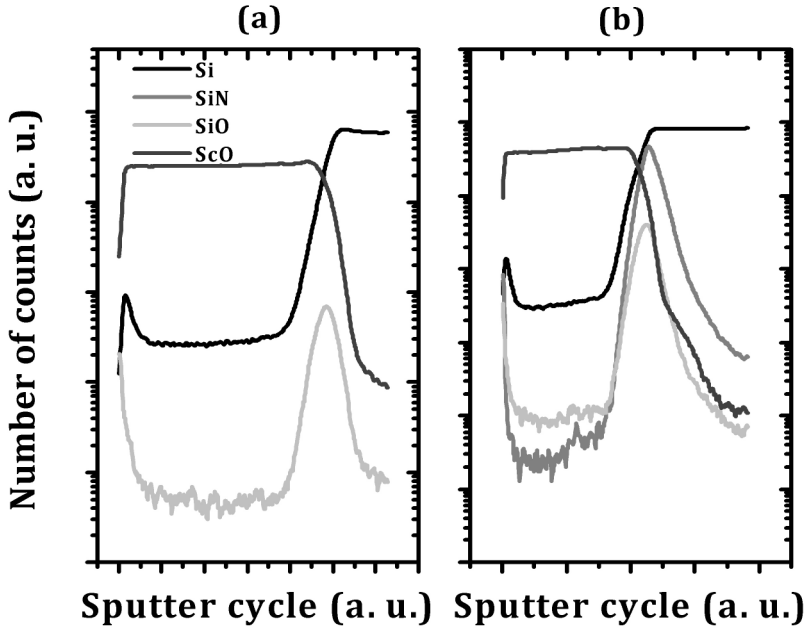

Figure IV.4 TOF-SIMS profiles of HPS deposited Sc_2O_3 on (a) H-terminated Si and (b) 10 min ECR nitrided Si.

The stoichiometry of the films was measured by XPS. The Sc 3d core-level spectrum of a representative sample is depicted in figure IV.5. The high resolution spectrum shows the spin-orbit splitting of 2p level with the $2p_{3/2}$ and $2p_{1/2}$ components at about 401.3 and 405.5 eV, respectively, which are characteristic of Sc_2O_3 [22]. The O 1s core-level spectrum shows an asymmetric shape which can be fitted to two components: a major one at 530.0 eV due to Sc-O-Sc bonds [22], and a minor one located at 531.6 eV, associated with OH^- groups adsorbed by the film surface, in a manner similar to other high κ materials [23]. A certain contribution to this last component could come from sub-surface O atoms. Taking into account only the Sc-O-Sc contribution, the O to Sc ratio is 1.4 ± 0.1 in all cases, regardless the substrate preparation. This is in agreement with GIXRD measurements, which showed a cubic bixbyite Sc_2O_3 phase in all samples.

TEM was used in order to determine the thicknesses of the layers and to confirm the previously shown results (poly-crystallinity and interface integrity). The most relevant images that were obtained are displayed in figure IV.6. Figure IV.6a shows a scandium oxide film deposited on an H-terminated Si surface. The image shows that a bright layer appears between two darker layers. The top dark

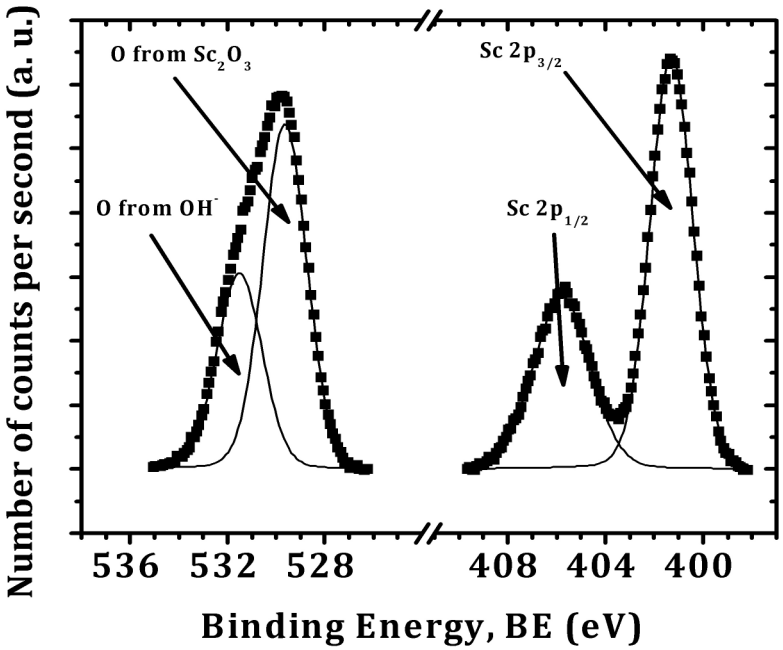

Figure IV.5 Representative XPS spectrum of the Sc_2O_3 films.

layer is the Sc_2O_3 film and the layer in the bottom is the Si substrate. The bright layer is silicon oxide that has been grown between the high κ dielectric and the Si and its thickness is about 1.7 nm. The formation of this layer could be explained by the O diffusion through the Sc_2O_3 film during growth. It must be noticed that SiO_x thickness is low, compared, for instance, with TiO_2 (that in similar conditions forms a ~6 nm SiO_x [24]) or HfO_2 (that presents a ~3 nm SiO_x [25]). This indicates that Sc_2O_3 blocks oxygen-radicals diffusion more effectively than TiO_2 or HfO_2.

The thickness of the Sc_2O_3 layer is around 30 nm, and the images confirm the poly-crystalline character of the Sc_2O_3 film. Additionally it is observed that the nano-crystals are randomly oriented, with no preferential growth direction, which is in agreement with GIXRD measurements. This is in contrast with previous HfO_2 results obtained with the same system [26], which showed a columnar growth. Finally, close to the interface the nano-crystals are not so clearly observed, suggesting an amorphous initial growth stage. These results show that if an amorphous layer was needed, for example as a gate dielectric, different HPS deposition conditions should be explored, like substrate temperature, target to substrate distance or *rf* power. Previous works [27] showed that HfO_2 films

deposited with Ar plasma were amorphous whereas deposited films with plasmas of O_2 or different Ar/O_2 ratios were poly-crystalline.

No significant differences in thickness or in poly-crystallinity are found for the Sc_2O_3 layer deposited on different substrates. Thickness spread is about 20%, which is not surprising due to the long deposition processes (2 h). The main differences lay in the Sc_2O_3/Si interface.

In figure IV.6b, the Sc_2O_3 film was deposited on a 30 s nitrided Si. We observe a 2.8 nm interface layer, which is SiN_x according to FTIR results. The interface film seems to present three-layer structure, but this should be a TEM artifact. In order to clarify this, TEM of the same sample was performed with a higher resolution microscope. Figure IV.6c shows this interface in more detail. The interface is

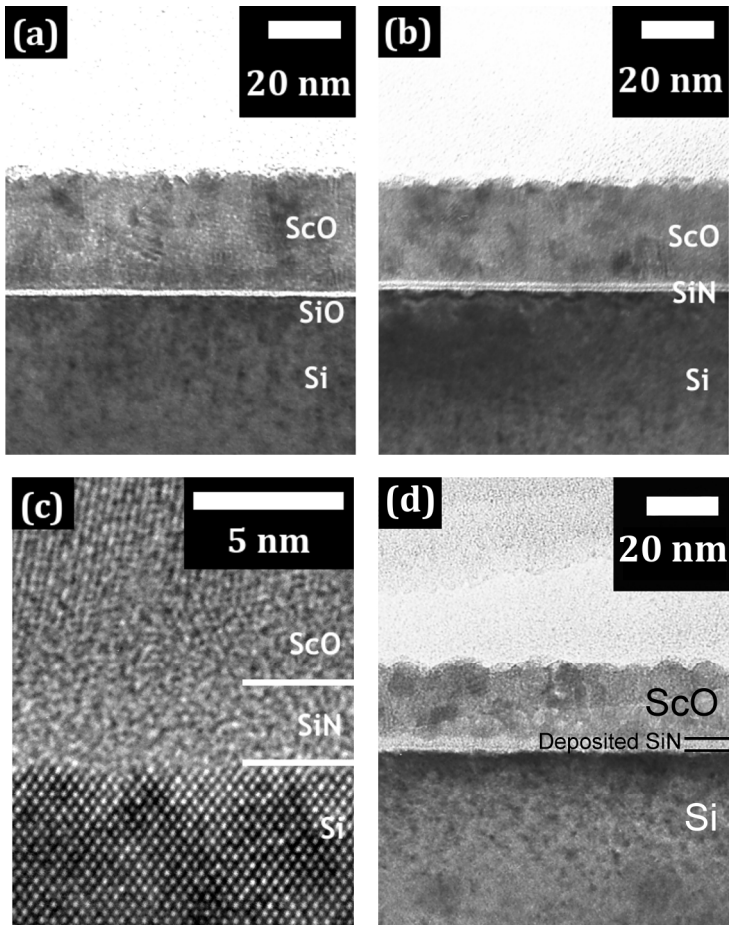

Figure IV.6 Cross-sectional TEM images of the Sc_2O_3 deposited films (a) on RCA after etching in a HF diluted solution and (b) on Si nitrided during 30 s. (c) Cross-sectional HRTEM image of a sample that consist in an interface (30 s nitridation) and Sc_2O_3 sputtering deposition. The thickness of the interface layer is 2.8 nm. (d) TEM image of Sc_2O_3 on deposited SiN_x/Si.

amorphous and homogeneous, with no observable differences as a function of depth, so the three-layer structure of the nitride can be discarded. In TEM images of deposited SiN_x (figure IV.6d), it is observed that a 3.5 nm thick silicon nitride layer has grown and its structure is also amorphous. From these results, together with FTIR and TOF-SIMS measurements, it is concluded that silicon nitride (either deposited or grown from Si) avoids Si re-oxidation during the initial stages of sputtering.

IV.2.2 ELECTRICAL CHARACTERIZATION

C_{QS} and C_{HF} curves as a function of V_G (at 100 kHz) were measured for the stacks with an Al gate. This measuring method is very reliable for D_{it} extraction, which is calculated from the difference between the high-frequency and the quasi-static curve in depletion. However, this technique needs MIS devices with very low leakage current. Otherwise C_{QS}-V_G curves are impossible to be measured in thin films. This means that thick insulator layers are needed, and it is the reason why around 30 nm thick Sc_2O_3 layers were used. Furthermore, for permittivity calculation, thick layers are less sensitive to interface thickness or dielectric inhomogeneities, since most of the capacitance is due to the high κ dielectric.

The most significant curves are shown in figure IV.7. C_{HF}-V_G curves have been analyzed by the Hauser algorithm [28]. The EOTs are too high for high performance applications but they are in the order used for blocking oxide or inter-poly-Si dielectric in flash memories.

Samples with silicon nitride interface have a higher capacitance in accumulation, which means an improvement of the EOT of the structure of 1.4 nm (from 13.1 to 11.7 nm). This is a consequence of the higher κ value of the SiN_x. Another interesting feature is the displacement of the flatband voltage of the devices with SiN_x (from 0.2 V to -0.3 V) which can mean trapped positive charges in the SiN_x layer [7]. As it was seen in the introduction to this chapter, these N-generated fixed charges near the channel are suspected to reduce electron mobility by Coulomb scattering. However, the pursuit of lower EOTs currently requires very thin SiO_2 interfaces, which also degrade carrier mobility. In this way, the nitridation of the interface may be less severe in terms of performance than further scaling of SiO_2 interface [7]. Besides, the devices with SiN_x interfaces show

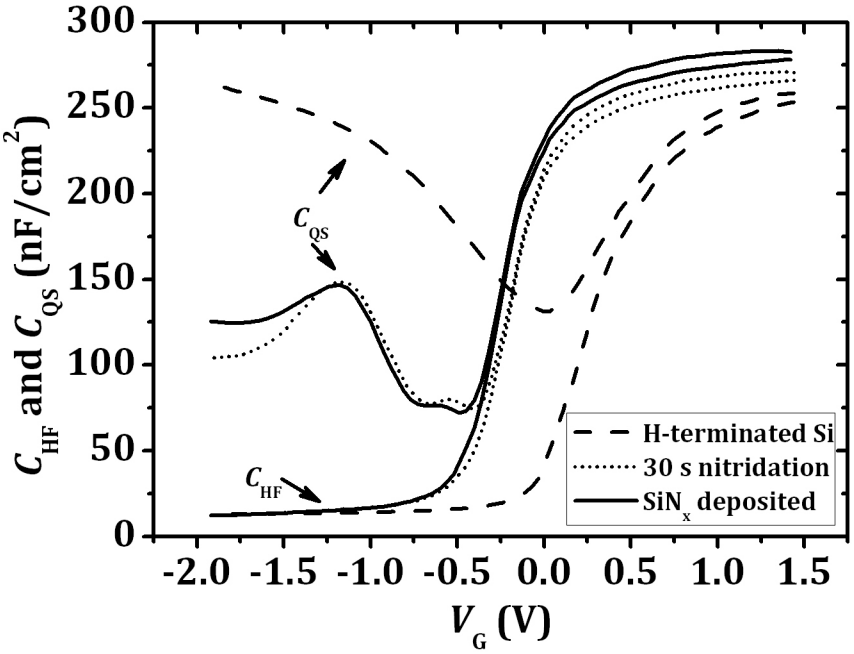

Figure IV.7 C_{QS} and C_{HF} characteristics of the stacks.

a much more abrupt decrease in the high frequency capacitance. This last effect exhibits an improvement in the interfacial density of states (high D_{it} has the effect of screening gate potential [29], producing a "stretch-out" of the C-V_G curve).

Nevertheless, when the SiN_x is present, the quasi-static capacitance in inversion does not recover its value of accumulation, which does not happen in samples with SiO_x as an interfacial layer. The reason of this effect is not completely clear. A possibility is that it can be associated to an intrinsic property of the interfacial SiN_x, but in the past, $HfO_2/SiN_x/Si$ stacks were grown that did not show this problem [10]. Another reason of such effect could be a higher gate leakage in inversion due to the smaller band gap of SiN_x compared to SiO_x. The leakage current density J_G-V_G curves of the stacks can be seen in figure IV.8. Samples with SiN_x interfaces present slightly higher leakages than those of samples with SiO-like interfaces at low inversion voltages, but all curves are close to the detection limit of the measurement system. These small differences are not supposed to explain by themselves the behavior of the quasi-static capacitance. Another possible explanation is that this effect is related to charge trapping centers, either in the SiN_x or in the Si surface. A similar behavior was found in previous works in SiN_x/plasma-oxidized-SiO_2/Si stacks [30], and it was found that after thermal

treatments the devices recovered the capacitance in inversion. In this way, since these MIS devices have only been subjected to a 300 °C FGA, it is likely that thermal annealing will improve their electrical behavior. All these effects are independent from the growth of silicon nitride: a deposition or a nitridation of the Si surface.

The dielectric permittivities of the deposited films were estimated by modeling the capacitance as two capacitors in series, where one is the interlayer and the other is the Sc_2O_3 deposition. For calculation, the interfacial layer is considered silicon oxide or silicon nitride, depending on the process of each wafer. Thus, the interlayer permittivity values κ_{IL} that were used were is 3.9 or 8 respectively. The thickness of the interlayer (t_{IL}) and of the Sc_2O_3 (t_{ScO}) were obtained from TEM images. Then, the Sc_2O_3 permittivity can be calculated as follows:

$$\kappa_{ScO} = \frac{t_{ScO}}{EOT/\kappa_{SiO} - t_{IL}/\kappa_{IL}} \qquad \text{equation IV. 1}$$

where κ_{SiO} is 3.9, silicon oxide permittivity. This way, as expected, all Sc_2O_3 films show a close permittivity value, with a mean value of 9 ± 1. This value is slightly lower than the bulk values reported in literature of about 13 [21]. This fact is usual for many thin film materials, but in our case Al might be reacting with the top Sc_2O_3

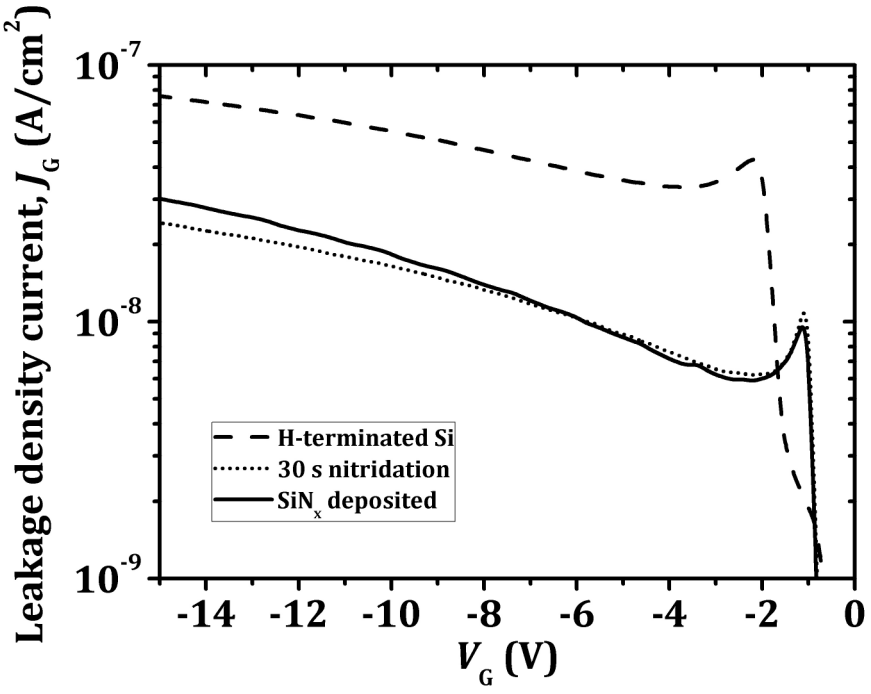

Figure IV.8 Gate leakage current in inversion of Sc_2O_3 deposited on different substrates as a function of gate bias voltage.

surface, forming an Al scandate and decreasing the effective permittivity [31]. However the aim of this experiment is the study of the Sc_2O_3/Si interface and the effect of the metal gate is analyzed in chapter VI.

Figure IV.9 depicts the D_{it} extracted from the C_{HF} and C_{QS}-V_G characteristics of figure IV.7. Thanks to the silicon nitride interlayer, the minimum in the D_{it} decreases from 10^{12} for the SiO_x/Si interface to 10^{11} eV^{-1} cm^{-2} for both deposited SiN_x or 30 s nitrided Si surface. The outcome of these measurements is that there is a significant improvement of the high κ dielectric/Si interface with nitride introduction. The D_{it} of the samples was also calculated by the conductance method at a frequency of 100 kHz. Table IV.1 summarizes the results of the two methods for the different substrates used in this experiment. Although conductance method tends to yield lower D_{it} values compared with the C_{HF} and C_{QS}-V_G method, it can be clearly observed that the tendency is the same for both methods and the presence of the SiN_x, either deposited or by nitridation of the Si surface, increases interface quality between the Sc_2O_3 and the Si.

Lastly, C_{HF}-V_G hysteresis curves of the MOS capacitors are shown in figure

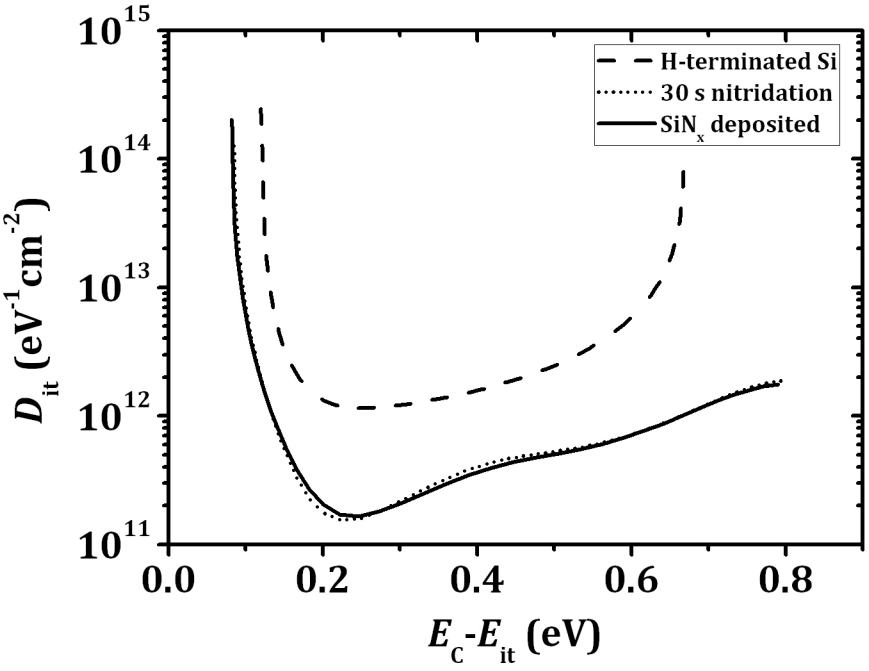

Figure IV.9 Density of interfacial defects D_{it} from C-V_G characteristics of figure IV.7 as a function interface trap energy measured from Si conduction band.

Table IV.1 Density of interfacial states D_{it} for different substrates obtained by the combined high-low frequency capacitance method and the conductance method.

Substrate	$D_{it,min}$ by C_{QS}-C_{HF} method (eV^{-1} cm^{-2})	D_{it} by conductance method at 100 kHz (eV^{-1} cm^{-2})
Native SiO_2 on Si	1.9×10^{12}	7.4×10^{11}
HF-etched Si	1.2×10^{12}	6.7×10^{11}
600 s nitrided Si	4.2×10^{11}	2.6×10^{11}
30 s nitrided Si	1.6×10^{11}	6.7×10^{10}
30 s deposited SiN_x on Si	1.7×10^{11}	1.4×10^{11}

IV.10. RCA native oxide devices present a remarkably high flatband shift ΔV_{FB} of 0.7 V. On the other hand, the H-terminated substrate presents a very small shift. When the curve is measured from accumulation to inversion, the sample with RCA native oxide interface presents a V_{FB} similar to the case of H-terminated Si substrate. Thus, the V_{FB} of the curve measured from inversion to accumulation is shifted because of positive charges that are trapped in the chemical oxide when the gate bias is negative. On the other hand, hysteresis curves show that the interfacial SiN_x layer avoids the shift in the V_{FB}, which indicates again a better quality of the interface.

IV.3 Summary and conclusions

In this chapter, conclusions were drawn about scandium oxide as a high κ dielectric and its interface with Si.

The compatibility of the Sc_2O_3 as a high κ dielectric with different substrates (bare Si, SiO_x and SiN_x) was studied. Sc_2O_3 potentially fulfils some important requirements of flash memory applications as has been demonstrated in this chapter. HPS deposited Sc_2O_3 films are poly-crystalline with no preferential growth direction. The composition of the layer is stoichiometric (from XPS measurements) and does not depend on the distance to the substrate (from TOF-SIMS). It is demonstrated that the physical properties of the Sc_2O_3 films are independent from the substrate preparation. The dielectric constants of the films are around 9.

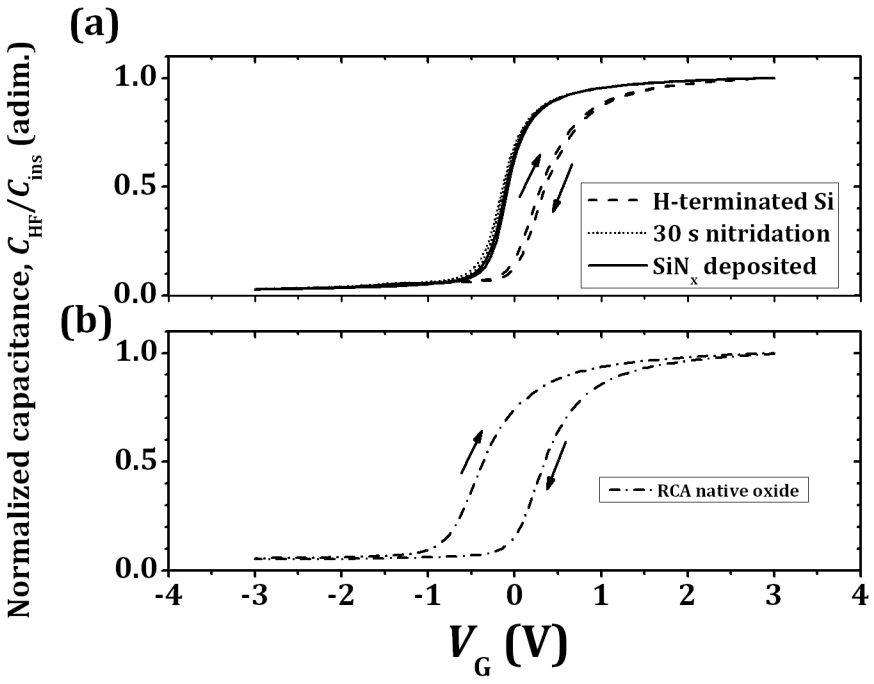

Figure IV.10 C_{HF}-V_G hysteresis curves (a) H-terminated Si, 30 s nitridation and 30 s deposited SiN_x, (b) RCA native oxide.

On top of that, concerning interfacial layer, it was checked that nitrided silicon or deposited SiN_x have several advantages over chemical/native SiO_2: it has a higher dielectric constant than SiO_2 which reduces the EOT of the structure; the interface is better than Sc_2O_3 deposited on H-terminated silicon or chemical SiO_2 (the minimum of the D_{it} improves one order of magnitude); it avoids O diffusion from the plasma that could oxidize Si surface. Besides, nitrided samples and deposited SiN_x proved to present a negligible flatband voltage shift in hysteresis measurements. These advantages encourage continuing with the study of silicon nitride as high κ dielectric/Si interface.

This way, we showed that SiN_x is a solution in case of poor interface quality and/or excessive SiO_x regrowth for HPS deposited Gd and Sc based oxides. However, we must keep in mind that introducing a SiN_x thin film imposes a penalty on the minimum EOT attainable. Thus we study the direct deposition of the high κ dielectrics on the H-terminated Si in the next chapters, and we keep the SiN_x interface as an open option.

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CHAPTER V. SCANDIUM OXIDE FILMS

Scandium oxide can play a role in the next generation of silicon transistors and memory devices. This material has a band gap of 6 eV [1] and a relative permittivity of 13 [2] that make it suitable for flash memory applications [3]. It can be used for electrical isolation between the control gate and the charge storage layer for both floating gate memories (*flotox*) and charge trapping memories. In *flotox* memories, the insulator is sandwiched between the poly-Si gates [4] and is called *inter-poly-Si dielectric*. In charge trap memories, the insulator or *blocking oxide* lies in contact with a silicon nitride trapping layer and a p-type metal [5]. Also, ternary based compounds such as $GdScO_3$, $DyScO_3$ and $LaScO_3$ have attracted interest in CMOS circuits because of their high permittivity and good stability in contact with Si [6, 7, 8].

In addition to this, Sc_2O_3 thin films find applications in several fields like e-beam lithography resist [9], damage resistant layer [10], antireflection coatings in light emitting diodes and high power ultraviolet lasers [11, 12], constituent of ferroelectric thin films [13], etc.

Up to the moment, Sc_2O_3 thin films with good properties are successfully deposited by Atomic Layer Deposition (ALD) [14, 15], although a wide variety of precursor gases are under study and no universal solution has been found. Moreover, an important drawback is the complexity of controlling the precursor fluxes. They should guarantee the completeness of the involved reactions. To produce a relatively thick film by ALD, a high amount of precursor gases must be consumed, and their fabrication includes environmental hazards. Furthermore, although it is rarely mentioned, the ALD films present a high amount of contaminants (typically carbon or chlorine) depending on the precursor chemistry that can be the origin of reliability issues [16].

In this chapter, we characterized deposition of ScO_x films by high pressure sputtering (HPS) on silicon under different conditions. We investigated the morphology, composition and crystal structure of the films by means of transmission electron microscopy (TEM), and Fourier transform infrared spectroscopy (FTIR). Ellipsometry determined the thicknesses of the films. We

fabricated metal-insulator-semiconductor (MIS) devices to analyze the electrical properties of ScO_x and its interface with the Si.

V.1 EXPERIMENT

Scandium oxide films were grown on two different kinds of substrates. For structural characterization, double side polished Si wafers with a resistivity of 200-1000 Ω cm were used. For electrical characterization, metal/ScO_x stacks were deposited on single side polished Si wafers with a resistivity of 1.5-5.0 Ω cm. In both cases the wafers were n-type doped with phosphorus (n-type Si) and the top surface corresponded to (100) plane. Native SiO_2 was removed from the surface by immersing the wafer in HF (1:50) for 30 s just before deposition.

ScO_x layers were deposited by HPS in a pure Ar atmosphere, using several conditions of pressure and radio frequency (*rf*) power. Prior to deposition, the base pressure was around 1-2×10^{-6} mbar while the pressures of the processes ranged from 0.25 to 1.3 mbar. A commercial 4.5 cm diameter high purity Sc_2O_3 target was used. The 13.54 MHz *rf* power was changed from 30 to 50 W. Depositions were performed for 30 min maintaining a constant substrate temperature of 200 °C.

MIS devices of areas ranging from 50×50 to 630×630 μm^2 were fabricated on the low resistivity substrates. The gate electrode square openings were defined with a lithography process (using the negative photoresist *n-LOF 2035*). Afterwards, 130 nm thick Al metal electrodes were deposited by e-beam evaporation, followed by the lift-off of the photoresist. A 150 nm thick Al layer was evaporated on the backside to obtain the substrate ohmic contact. After fabrication, samples were annealed in forming gas (FGA) during 20 min at 450 °C for the passivation of interfacial defects.

FTIR spectra of the samples were measured in the 4000-400 cm^{-1} region in order to analyze the bonding structure of the films and the interfaces. These spectra have been corrected by subtracting the spectrum of a bare Si substrate of the same lot to remove the substrate absorbance. The Si substrate was immersed in HF 1:50 for 30 s immediately before the FTIR measurement to avoid the native

oxide presence in the reference spectrum. Spectra have been shifted vertically for clarity.

Samples were also characterized by TEM and ellipsometry. The emission lines of the HPS glow discharge were registered for a better understanding of the growth. The capacitance and conductance of the MIS capacitors were measured as a function of the gate bias voltage. Finally, hysteresis curves were analyzed and related to the densities of interface defects, estimated by the conductance method.

V.2 RESULTS AND DISCUSSION

V.2.1 STRUCTURAL CHARACTERIZATION

In the first place, we remember the structural characterization of the ScO_x film from chapter IV (deposited for 2 h, at 0.50 mbar and 40 W), in order to compare it with the thin films grown in this experiment (deposited for 30 min). Those films were grown on the same kind of substrate that is used in this experiment (H-terminated Si). Figure IV.6a shows a cross sectional TEM image of this sample, where a ~34 nm thick poly-crystalline ScO_x layer is observed. However, this image also suggests an amorphous initial growth stage. A SiO_x interfacial layer of 1.7±0.3 nm appears between the high κ and the Si. The glancing incidence X-ray diffraction pattern of the sample is represented in figure IV.3b, which correspond to the Sc_2O_3 cubic bixbyite phase. No preferential direction in the growth is observed. These results are also supported by the TEM image in figure IV.6a.

The FTIR spectrum of the thick ScO_x film deposited on Si is depicted in figure V.1a, corrected with the spectrum of an HF-etched Si substrate. The wavenumbers above 1200 cm^{-1} do not show any relevant feature, and they have been omitted for clarity. In the figure, a peak at 667 cm^{-1} is found, which is related to residual CO_2 present in the camera [17], and two more at about 730 and 610 cm^{-1}, due to the phonon absorption of Si [18]. These last two peaks can be attributed to a small wafer thickness difference between the sample and the reference substrate. We observe a broad band at around 1070 cm^{-1} that corresponds with the Si-O stretching vibration, whose tabulated value is 1065 cm^{-1} [19, 20]. On the other hand, the increase in the absorbance in the 600-400 cm^{-1} region can be related to

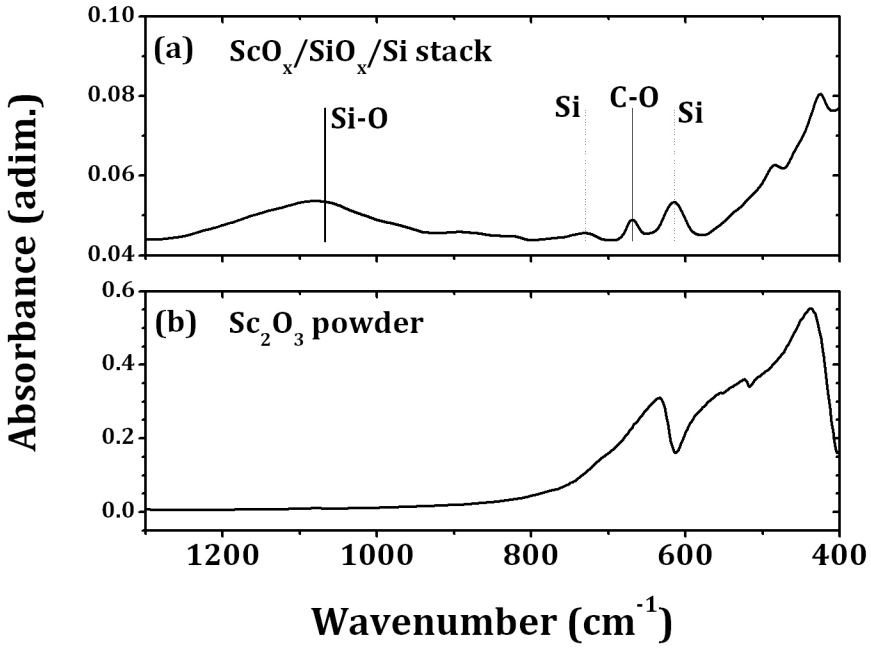

Figure V.1 (a) FTIR spectrum of the sample with a deposition of Sc_2O_3 at 0.50 mbar and 40 W for 2 h. It has been corrected with a HF-etched substrate. The increase of absorbance in the 500-400 cm^{-1} region is associated with the Sc-O bonds. (b) FTIR spectrum of Sc_2O_3 powder.

the Sc-O bonds, as literature shows [21] and as can be concluded from comparison with the measured spectrum of Sc_2O_3 powder, shown in figure V.1b. From these results, it is confirmed that a poly-crystalline ScO_x layer is deposited on Si, and an interfacial layer of SiO_x grows from the reaction with the substrate.

Now, we will explore the properties of the thin films deposited for 30 min with different conditions. Figure V.2 depicts the thicknesses of the ScO_x layers as a function of the *rf* power measured by ellipsometry. The high κ layers were grown at 0.50 mbar. As expected, higher powers yield thicker layers due to the increase in the energy of the particles in the plasma. The growth rate speeds up due to the rise in the amount of sputtered atoms. However, this increment is not linear, but tends to saturate at an *rf* power above 40 W. As a consequence, we fixed 40 W as working *rf* power in the following experiments, varying the deposition pressure.

In figure V.3, the thicknesses of the films grown for 30 min are represented for different deposition pressures. Firstly, we can observe that growth rate shows a maximum at 0.50 mbar and it decreases significantly for higher pressures. This trend was also found for HfO_2 growth in the same HPS system in an O_2 atmosphere,

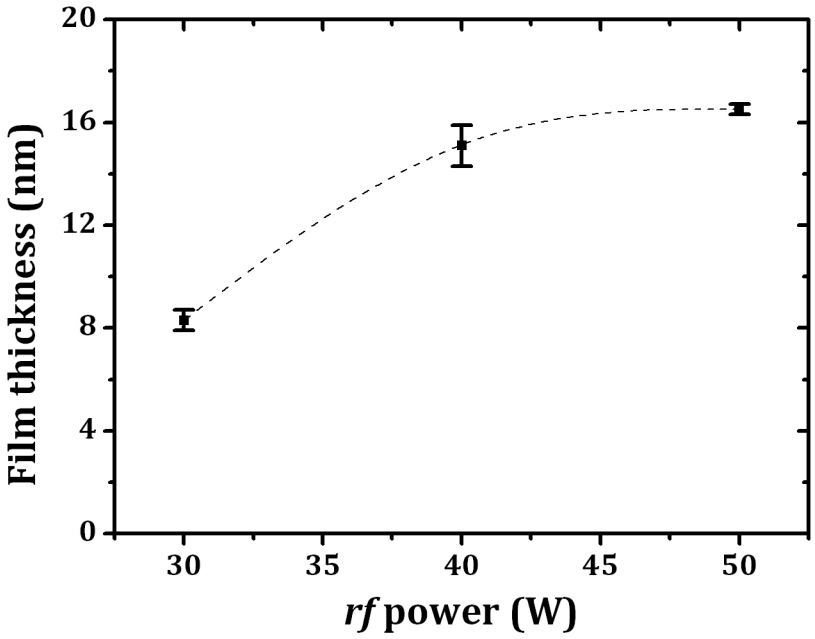

Figure V.2 Film thicknesses of the ScO_x films deposited in pure Ar atmosphere at 0.50 mbar during 30 min, measured by ellipsometry, as a function of the applied *rf* power.

with similar deposition conditions [22]. A rise in pressure shortens the mean free path and the diffusion length of the particles in the plasma. This reduces the flux of sputtered Sc and O atoms that reach the substrate. Znamenskii et al. found a similar dependence for high-pressure magnetron sputtering [23] and proposed a diffusion model for the thermalized atoms that is consistent with the results shown here.

Also, figure V.3 shows that for pressures below 0.5 mbar, the dielectric film grows at a slower rate. We explain this with the aid of the plasma optical spectra, which are represented in figure V.4. In this graph, neutral and singly-ionized Ar (Ar I and Ar II) are observed, regardless of the pressure [24, 25]. However, Sc I peaks [26] are under the detection limit for 0.25 mbar (only the doublet at 402.0-402.4 nm might be appearing) while they are present for higher pressures. A lower concentration of Sc would make the sputter rate decrease.

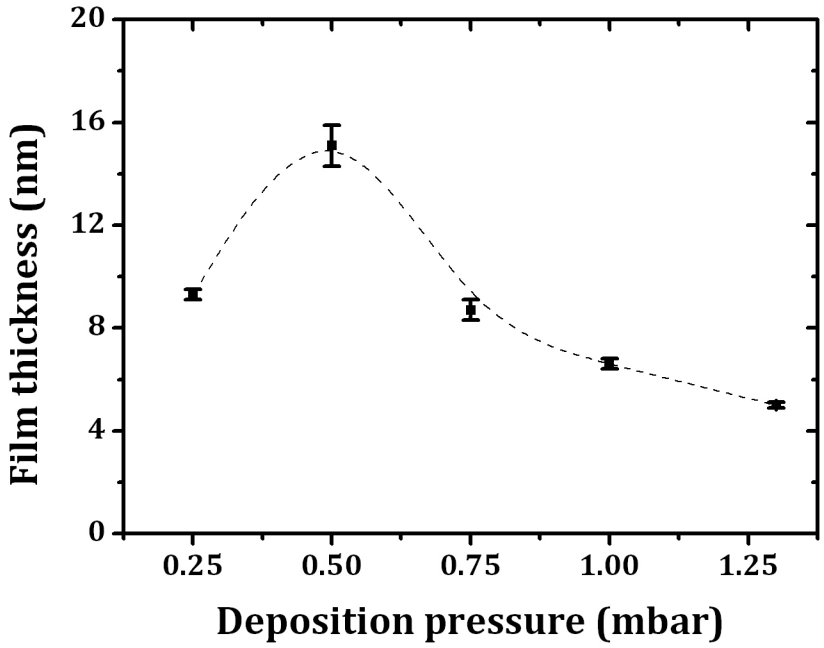

Figure V.3 Film thicknesses of the ScO_x layers for deposition pressures ranging from 0.25 to 1.3 mbar of pure Ar, at 40 W of *rf* power, during 30 min. Measurements were taken by ellipsometry.

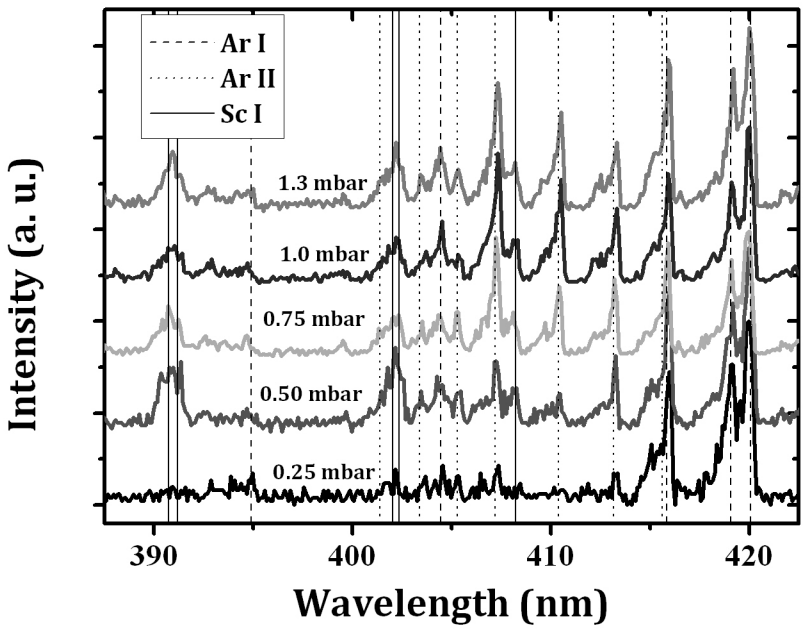

Figure V.4 Optical spectra of Sc_2O_3 sputtered at different pressures at 40 W of *rf* power. The most relevant peaks of Sc I, Ar I and Ar II are indicated by vertical lines. At 0.25 mbar, the peaks of Sc are under the detection limit.

These results show that growth rate has a maximum at 0.50 mbar and thus, the two effects compensate at around that pressure. In fact, the intensity of the Sc I emission in figure V.3 can be qualitatively correlated to the growth rate: its peaks at 0.50 mbar are the most intense of all spectra. However, direct correlation is difficult. Pressure changes the confinement of the plasma and thus the amount of photons that reach the aperture of the spectra acquisition system. In any case, the growth rate allows us to obtain nanometric-thick films in the order of minutes for all pressures. This way, we could control precisely the thicknesses of the layers.

FTIR spectra are represented in figure V.5a in the 1200-400 cm^{-1} region. These spectra do not present the broad peak at 600-400 cm^{-1} that was attributed to the Sc-O bond on the thicker layer, probably because of the lower thickness of these films. In the lowest wavenumber region, we can only appreciate the effects of the substrate correction. A band at around 1050 cm^{-1} appears mainly for deposition pressures below 0.50 mbar. It corresponds with the asymmetric stretching vibration mode of the O-Si-O unit. The shift towards lower wavenumbers with respect to the tabulated value [19] might be related to stress in the silicon oxide film, which is caused by the presence of sub-oxides near the Si/SiO_2 interface [27]. For deposition pressures above 0.75 mbar, this band is less intense. In figure V.5b the area of Si-O band is depicted versus the deposition pressure and *rf* power. In FTIR measurements, the area of a peak is proportional to the concentration of associated bonds [28]. Thus, these graphs suggest a thinner SiO_2 interlayer for high pressures and for lower *rf* powers. In the following section we will discuss the influence of this interfacial layer on the density of interfacial defects and on the hysteresis of the C_{HF}-V_G curves.

Now, we analyze the influence of the FGA process. Figure V.6 shows the spectra of 14 nm and 43 nm thick ScO_x films deposited at 0.50 mbar of pressure and 40 W of *rf* power, before and after the FGA at 450 °C. The thicker ScO_x film presents a thicker interfacial SiO_x. Then, a longer deposition time produces a thicker interfacial SiO_x. We conclude that the SiO_x grows during ScO_x deposition. However, as it is known from growth dynamics [29], this SiO_x growth is not linear. FTIR results confirm this, since the SiO_x peak area is only ~25% smaller for the thinner film, in which the ScO_x is three times thinner. We also find that the Si-O

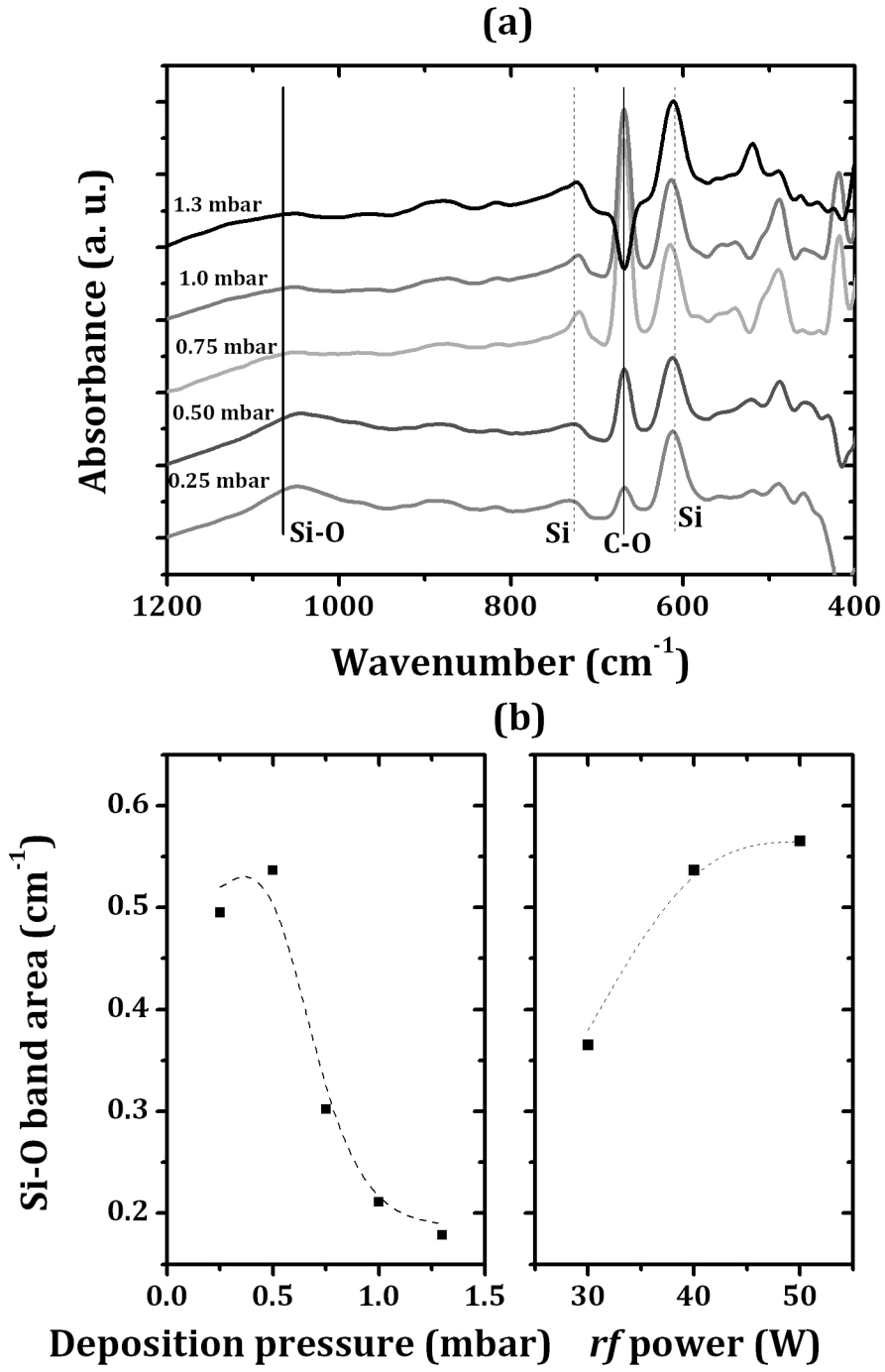

Figure V.5 (a) FTIR spectra of ScO_x layers deposited at pressures ranging from 0.25 to 1.3 mbar of pure Ar, at 40 W of *rf* power, during 30 min. The indicated absorption band (1065 cm^{-1}) corresponds to the SiO_2 bond stretching vibration. (b) Si-O band area as a function of the deposition pressure at 40 W of *rf* power (left) and of the deposition *rf* power at 0.50 mbar of pressure(right). Dashed lines are drawn as a guide to the eye.

band increases after the FGA. The inset in figure V.6 depicts the increment of the band area caused by the annealing. The FGA process prompts a regrowth in the interfacial SiO_x, most likely activated by residual O_2 present in the film or the FGA furnace.

Finally, figure V.7 shows the structure of an Al gated MIS capacitor after the FGA at 450 °C, where we observe the different layers of the stack. The high κ dielectric was grown at 0.50 mbar. This layer is much thinner than the one in figure IV.6a and it looks completely amorphous. Also, a 3.3±0.3 nm thick SiO_x layer appears in the ScO_x/Si interface. The contrast in the upper part of the ScO_x film suggests that the Al gate is reacting with the dielectric layer, as it has been previously referred [30]. The thickness of the interface layer is comparable with previous results obtained with HfO_x deposited in similar conditions [31] which also presented a ~3 nm SiO_2 interface. We can compare this interface with the 1.7 nm layer observed in the image of figure IV.6a, taken before the FGA. The annealing may be increasing the SiO_x thickness. In addition to this, the formation of an Al scandate ($AlScO_x$) might decrease the effective permittivity of the stack [30]. Both effects could influence the capacitance in accumulation C_{ins}, as it will be seen in the next section.

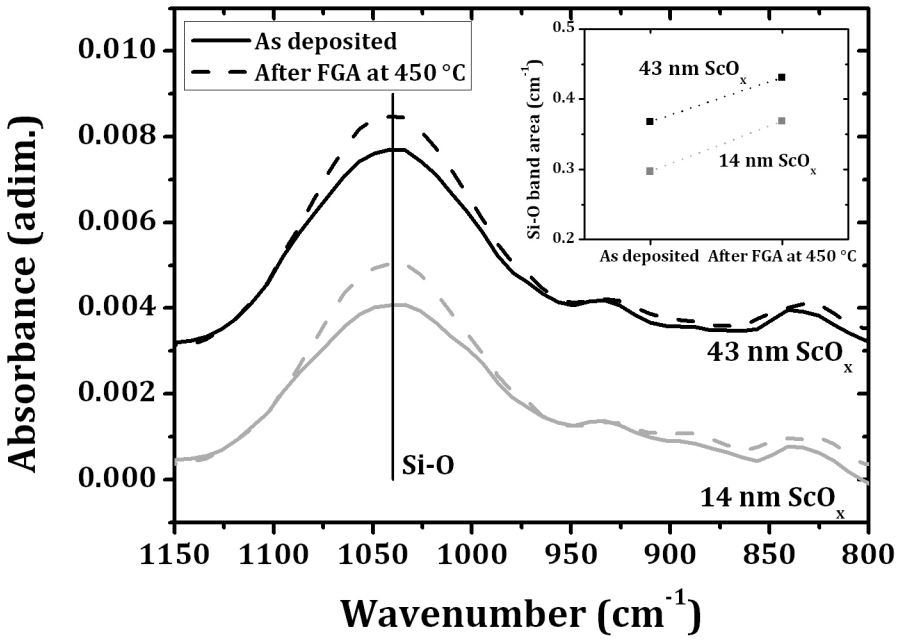

Figure V.6 FTIR spectra of 14 and 43 nm thick ScO_x layers grown at 0.50 mbar and 40 W before (solid lines) and after the FGA process (dashed lines). In the inset, the area of the Si-O stretching vibration peak (around 1050 cm^{-1}) is represented before and after the annealing.

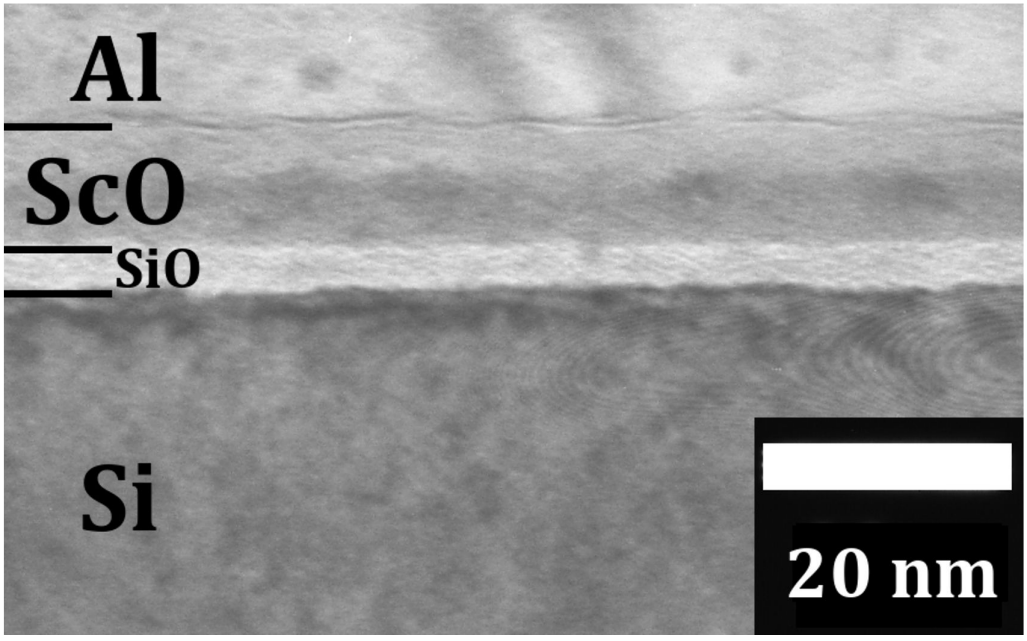

Figure V.7 TEM image of an Al/ScO_x/SiO_x/Si stack. ScO_x film was deposited at 0.50 mbar and 40 W. After metallization, sample went through a FGA process at 450 °C for 20 min.

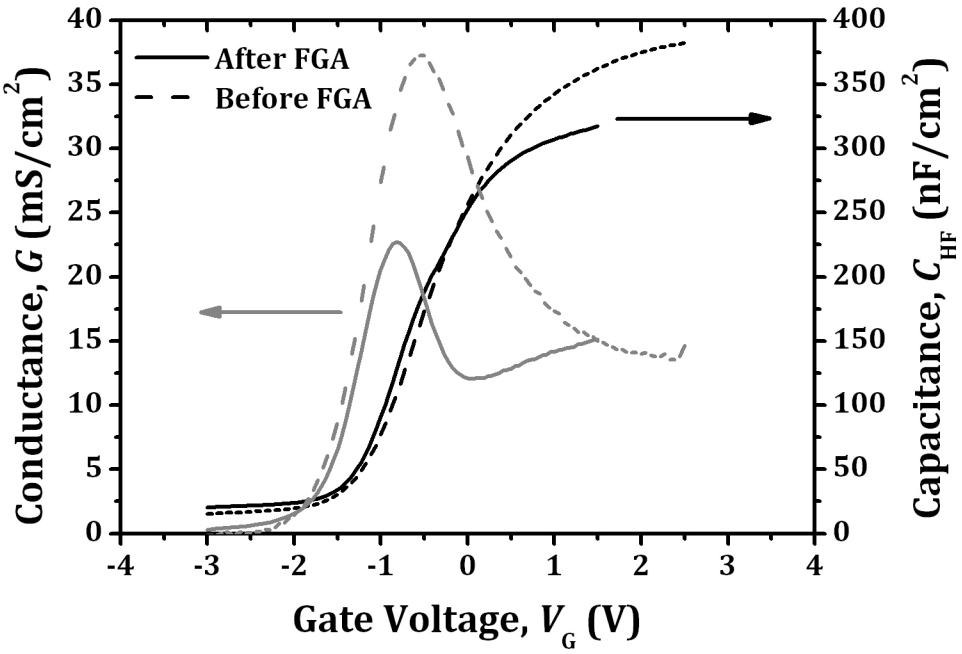

Figure V.8 C_{HF}-V_G and G-V_G curves of the sample deposited at 0.50 mbar and 40 W for 30 min, before (solid lines) and after the FGA process (dashed lines).

V.2.2 ELECTRICAL CHARACTERIZATION

We represent the C_{HF}-V_G and G-V_G characteristics at 100 kHz of the sample deposited at 0.50 mbar and 40 W for 30 min before and after FGA in figure V.8. Non zero values of the conductance G are associated with small-signal energy loss. The energy loss presents a peak whose main source is the interfacial traps. Although series resistance must be taken into account, a larger conductance peak would roughly mean a larger density of interface defects. Figure V.8 shows that after the FGA, both C_{ins} and the conductance are reduced. The decrease in the conductance can be associated to a decrease in the D_{it}, as has been discussed. This is caused by the passivation of the dangling bonds in the SiO_x by H atoms during the FGA process. Regarding the decrease in the C_{ins}, it is observed that the equivalent oxide thickness (EOT) of the MIS capacitor rises from 8.5 nm to 10.0 nm after the FGA. The 1.5 nm increment of the EOT points to the growth of the interfacial layer that is suggested by the FTIR results (figure V.6). The presence of an $AlScO_x$ (figure V.7), which has a lower permittivity than Sc_2O_3, would also influence this value. This could be avoided by selecting a different metal gate electrode, and will be further discussed in following chapter.

Figure V.9 shows the C_{HF}-V_G hysteresis curves at 100 kHz of MIS devices with ScO_x deposited for three representative deposition pressures and the same *rf* power, 40 W. We measured the curves starting in accumulation. For pressures below 0.50 mbar, samples present a significantly high flatband voltage shift, ΔV_{FB}, of around 0.5 V. This indicates charge trapping in the oxide defects due to the gate voltage applied to the device. Nevertheless, layers deposited at higher pressures have much lower shifts. Figure V.10 represents the ΔV_{FB} versus the deposition pressure and *rf* power. If this figure is compared with the interfacial SiO_x thickness of figure V.5b, we find a direct correlation between the thickness of the interfacial layer and the flatband voltage shift. This indicates that the un-intended SiO_x layers are very defective, and the charge and discharge of the traps during the hysteresis curve produces the flatband shift. However, when the SiO_x film is thinnest, there is almost no hysteresis, which means that the scandium oxide is much less defective than the SiO_x. These results highlight the advantages of sputtering at higher pressures, and encourage the use of HPS Sc_2O_3 as inter poly-Si layer in flash

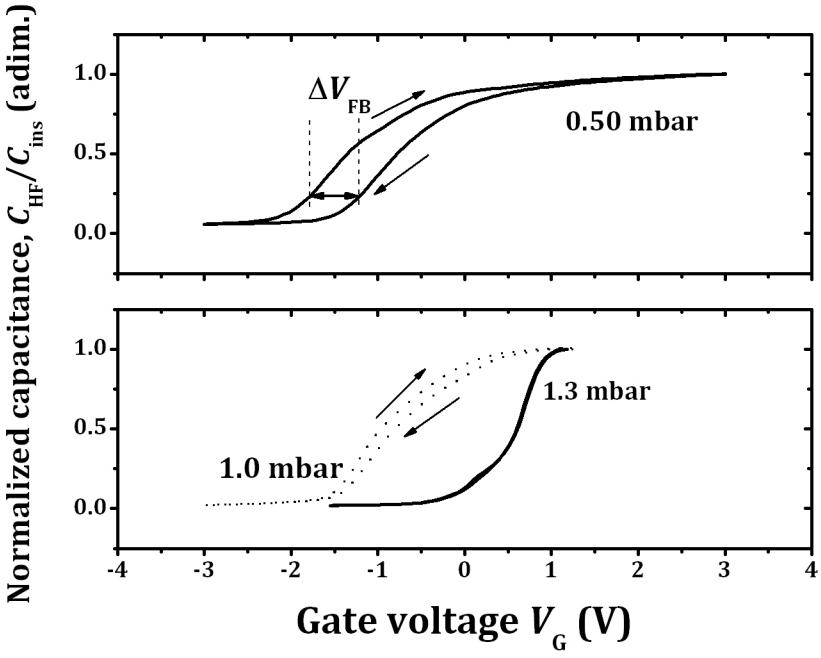

Figure V.9 Representative C_{HF}-V_G hysteresis curves of samples deposited at several pressures. For higher pressures, flatband voltage shift is lower.

memories, since for this application the minimized amount of defects is very important [3].

Finally, we estimated the density of interfacial defects D_{it} by the conductance method at a frequency of 100 kHz. The results are presented in figure V.11. As expected, FGA consistently reduces the density of defects by a factor of ~2. Also, the density of interfacial defects decreases with increasing deposition pressure. This indicates that higher pressures produce less damage to the Si surface, likely during the first stages of the ScO_x growth. This is again due to the reduced reactivity of the plasma in the high pressure regime. Then, the density of defects on HPS-grown ScO_x is low and thus remote phonon scattering is acceptable. We will see this again when further discussing the ScO_x/Si interface in chapter VII [32].

V.3 Summary and conclusions

We have explored structural and electrical characterization of ScO_x thin films grown by HPS. We observed that, for long deposition times (2 h), a thick poly-crystalline Sc_2O_3 layer is deposited, with no preferential direction of growth and that reacts with the Si substrate to form a SiO_x interfacial layer. Special insight was provided about the kinetics of this interlayer and its relation with the deposition

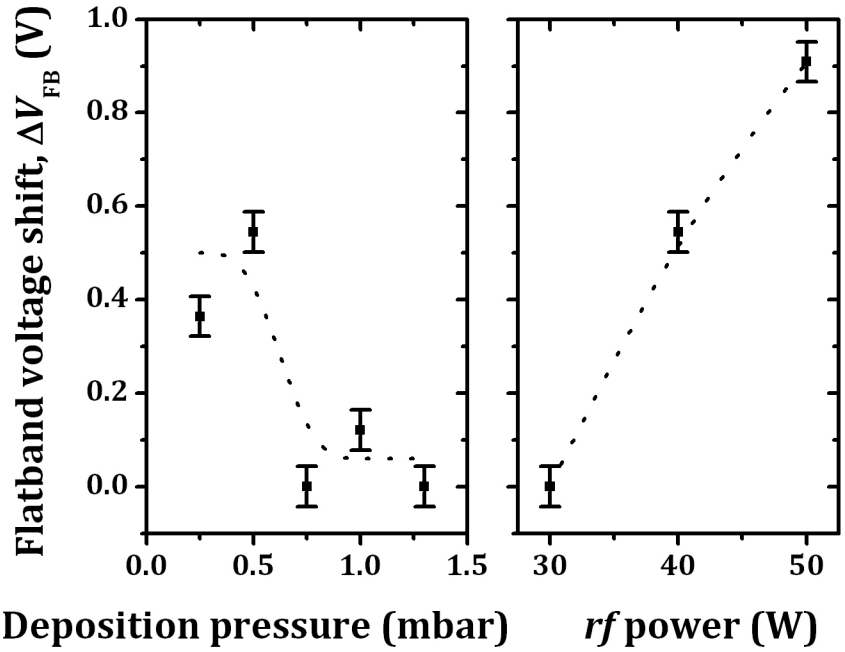

Figure V.10 Flatband voltage shift for Al/ScO_x/SiO_x/Si MIS devices deposited at (a) different pressures and (b) different *rf* powers. Dotted lines are drawn as a guide to the eye.

pressure and *rf* power. FGA process passivates the SiO_x interface, decreasing the density of defects, but it also may affect the EOT by forming an interface SiO_x layer or $AlScO_x$. Sputtering at high pressures (above 1.0 mbar) reduces the interfacial SiO_x formation, according to FTIR spectra. The devices fabricated with ScO_x deposited at high pressures present lower flatband voltage shifts in the C_{HF}-V_G hysteresis curves and lower density of interfacial defects. With this, we showed the advantage of high pressure conditions in reducing the plasma damage of the substrate. On the other hand, growth rates are slower for higher pressures, which will permit an accurate control of the thickness of thin layers.

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CHAPTER VI. GADOLINIUM OXIDE FILMS

Gadolinium oxide has been widely proposed as an interesting high permittivity gate dielectric for applications in flash memory devices and CMOS transistors [1, 2, 3]. It has drawn attention as a high κ material based on thermodynamic considerations and good insulating properties: gadolinium oxide has a permittivity value κ around 14, a band gap around 5.3 eV, and very good thermal stability with Si [2, 4]. Several papers reported high κ Gd_2O_3 films grown on Si substrates by electron beam evaporation or atomic layer deposition, with promising results [1, 5, 6]. Gd_2O_3 thin films are also used as passivation layers in III-V substrates [7, 8], waveguides [9], buffer layers in superconductors [10] and scintillating films [11], protective coatings [12], etc. Therefore, the study of the growth of this material can help in these applications.

This chapter deals with electrical and structural analysis of gadolinium oxide films grown on Si by high pressure sputtering (HPS) [13]. We used transmission electron microscopy (TEM), glancing incidence X-ray diffraction (GIXRD), X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared spectroscopy (FTIR) for structural characterization. We fabricated metal-insulator-semiconductor (MIS) devices with Ti and Pt gates to study the electrical properties and the influence of the choice of the metal electrode.

VI.1 EXPERIMENT

For structural characterization, gadolinium oxide thin films were grown on 2-inch double side polished n-Si (100) wafers with a resistivity of 200-1000 Ω cm. MIS devices were fabricated on single side polished 2-inch n-Si (100) wafers, with a resistivity of 1.5-5.0 Ω cm. Before high κ GdO_x deposition, substrates were cleaned using a standard RCA clean and submerged in a diluted HF solution (1:50) to remove all SiO_2 from the surface just before introduction to the sputtering chamber.

GdO_x films were deposited by HPS from a 4.5 cm diameter high purity Gd_2O_3 target in a pure Ar atmosphere. The 13.54 MHz radio frequency (*rf*) power was 40 W. Deposition pressures ranged from 0.50 to 1.3 mbar to study the effect of the

Ar pressure on the properties of the high κ dielectric. Base pressure was 1-2×10^{-6} mbar, five orders of magnitude below working pressure, to minimize contamination. Substrate temperature was maintained at 200 °C during growth. The deposition time was fixed at 30 min to obtain nanometric thick films. Also a thicker sample was grown during 2 h at 0.50 mbar to increase signal in the structural characterization. Optical spectra of the plasma at the different Ar pressures were acquired to analyze the changes in the emission of the excited species in the plasma.

MIS devices were fabricated for high frequency (HF) capacitance as a function of gate voltage (C_{HF}-V_G) measurements. The gate electrodes were 100 nm of Ti on one half of each wafer or 16 nm of Pt on the other half. Both metals were capped by 200 nm of Al, in the Ti case to avoid surface oxidation, and in the Pt case to minimize series resistance and to prevent dielectric perforation while probing. All these metals were deposited by e-beam evaporation with the other half of the wafer shadowed. This way it is assured that for each deposition condition the high κ dielectric is identical and differences can be attributed only to the metal electrode properties. Squares of different sizes ranging from 50×50 to 630×630 μm^2 were defined by a lift-off procedure. Then, a 300 nm thick Al layer was evaporated on the backside to obtain the substrate ohmic contact. After fabrication and electrical characterization, samples were annealed at 450 °C in forming gas (FGA process) for 20 min and characterized again electrically and by TEM.

We studied the physical properties of the films through ellipsometry, TEM, GIXRD, XPS and FTIR. FTIR spectra were measured in the 4000–400 cm^{-1} region and were substrate corrected with a spectrum of a bare Si substrate, previously immersed in HF 1:50 for 30 s to remove SiO_x from the surface. Energy-dispersive X-ray (EDX) spectrometry was used during TEM image acquisition to determine the species present in the thin films. C_{HF}-V_G and G-V_G curves were obtained at 100 kHz. Density of interfacial defects D_{it} was estimated by the conductance method [14].

VI.2 RESULTS AND DISCUSSION

VI.2.1 STRUCTURAL CHARACTERIZATION

In the following the physical properties of the gadolinium oxide films are studied as a function of the deposition pressure. The *rf* power was chosen as 40 W since it was the *rf* power used for the scandium oxide studied in chapter V. The ScO_x growth rate increases with *rf* power up to 40 W and it saturates for higher pressures. This power was chosen in order to obtain a reasonably high growth rate while minimizing substrate damage.

Figure VI.1 represents the optical spectra of the Ar plasma sputtering the Gd_2O_3 target in the 385-425 nm region for different Ar pressures. This technique allowed us to determine the optimal growth pressure range of the Gd_2O_3 films. No water or N_2 is found in the plasma, which is an indication of the absence of gas leaks. No oxygen signal is found in the plasma spectra but Toledano *et al.* also observed this fact when sputtering HfO_2 in an HPS system [15]. They produced stoichiometric films, which indicates that the O peaks absence should not be an issue. The Gd I peaks are under the detection limit for pressures below 0.50 mbar (for instance, at 387 nm and 423 nm), as it happened with the Sc lines from the Sc_2O_3 target (chapter V). Then, we chose the growth pressures from 0.50 to 1.3 mbar to guarantee the presence of Gd atoms in the plasma. For higher pressures, the plasma instability in the HPS chamber can jeopardize reproducibility of the growth. It is noteworthy that this pressure range coincides with the ScO_x case. This is positive, since to grow the gadolinium scandate the working pressure is the same for both targets (chapter VII).

Once that the pressure range is fixed, we discuss the structural characterization of a thick Gd_2O_3 film (grown on H-terminated Si at 0.50 mbar and 40 W during 2 h). According to ellipsometry, this film possesses a thickness of 190 nm and a refractive index of 1.9. The obtained refractive index is consistent with literature, in the range of 1.8-2.0 [16]. The growth rate is about 1.6 nm/min and it is significantly higher than for ScO_x, for which a 34 nm film is obtained for a 2 h deposition with the same pressure and *rf* power conditions. This means that the sputter yield is about 4 times higher for the Gd_2O_3 than for the Sc_2O_3 target.

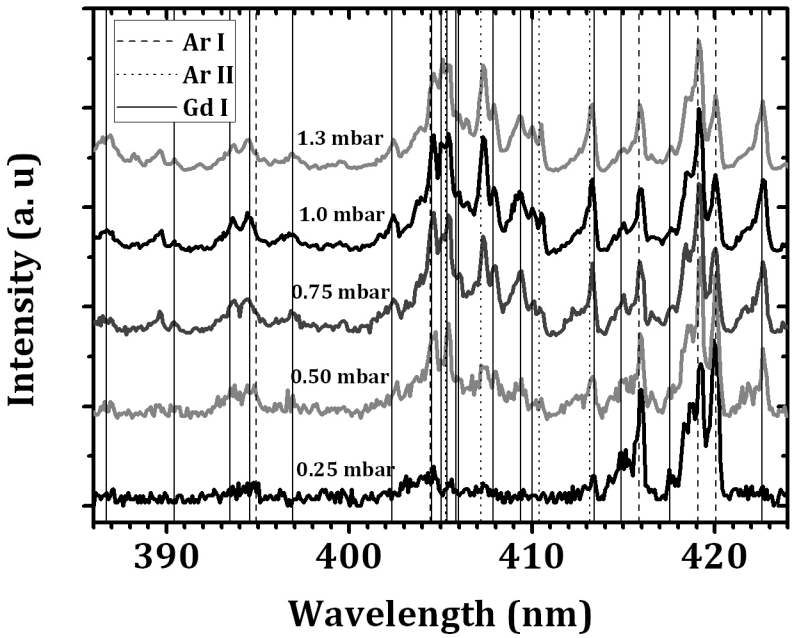

Figure VI.1 Plasma spectra of Gd_2O_3 sputtered at different Ar pressures and 40 W of *rf* power. The most important peaks of Gd I, Ar I and Ar II are denoted by vertical lines. Gd I peaks are not detected for pressures below 0.50 mbar.

Figure VI.2a shows the FTIR spectrum in the 1300-400 cm^{-1} region and it can be compared with the spectrum of pure Gd_2O_3 powder shown in figure VI.2b. In 667 cm^{-1}, the C-O bond peak appears due to residual CO_2 gas present in the measurement chamber. The valleys at 730 and 610 cm^{-1} are related to the crystalline Si vibration modes and are due to the small thickness differences between the sample wafer and the substrate used for correction. The small band at around 1050 cm^{-1} is attributed to the transversal optic vibration of the Si-O bond [17], which should appear at 1065 cm^{-1} for fully stoichiometric relaxed SiO_2. In the inset of figure VI.2a, we compare this band to the Si-O band that is formed under ScO_x deposition, at around 1070 cm^{-1} (from the figure V.1). It it is much less intense for the gadolinium oxide, which suggests that the Gd_2O_3 produces an interface SiO_x layer thinner than the ScO_x. Besides, the shift towards lower wavenumbers in the case of the Gd_2O_3 deposition could be associated with the presence of a Si rich SiO_x or a stressed SiO_2 layer [18, 19]. The bond formation with Gd, which has a much higher atomic mass than Si, would also shift the Si-O-Si band towards lower wavenumbers [20]. In chapter VII, we compare the interface layers of Gd_2O_3, Sc_2O_3 and $GdScO_3$ with Si. Figure VI.2a also shows peaks at around 529 and 451 cm^{-1} that

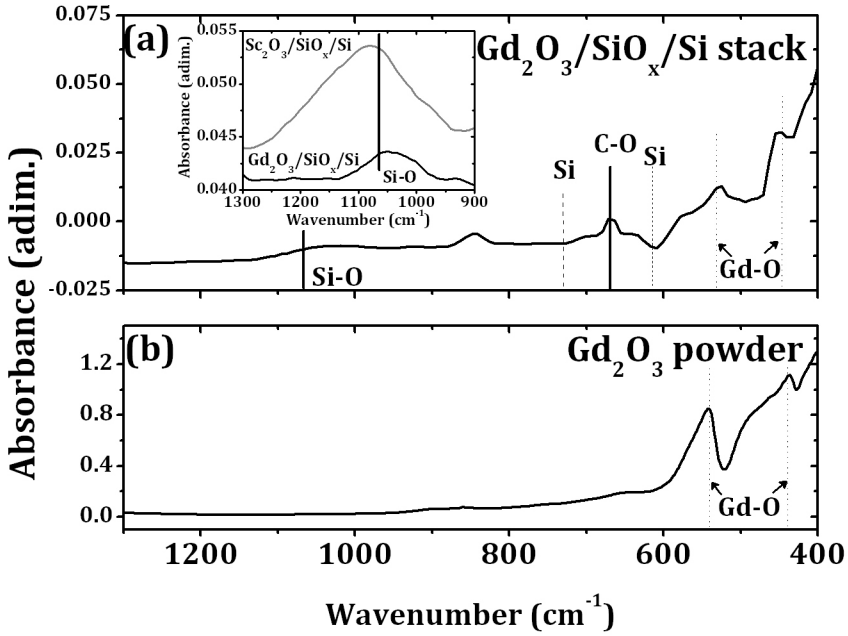

Figure VI.2 (a) FTIR spectrum of the 190 nm thick Gd_2O_3 on Si after substrate correction. The inset is a comparison between the Si-O band for the Gd_2O_3 and the Sc_2O_3 samples. (b) FTIR spectrum of Gd_2O_3 powder.

can be assigned to the Gd–O vibrations. We can infer it from direct comparison with the Gd_2O_3 powder spectrum shown in figure VI.2b. Other works also reported peaks at 538 and 456 cm^{-1} that are associated to Gd-O vibrations in the cubic Gd_2O_3 phase [21, 22, 23].

The GIXRD pattern of the thick unannealed Gd_2O_3 layer is depicted in figure VI.3. It clearly shows the most intense diffraction peaks of the cubic Gd_2O_3 structure [24]. Since all cubic diffraction peaks are found, with the relative intensities matching the theoretical calculations, these results point to a poly-crystalline structure with no preferential growth direction. The GIXRD spectrum evidences that the gadolinium oxide is poly-crystalline as deposited by the HPS, in other words, without any further annealing.

Summarizing, from these structural measurements we conclude that, as it is usual when depositing high κ dielectrics on Si, the 190 nm film consists of a poly-crystalline phase of cubic Gd_2O_3 that grows with no preferential direction, and that an interface SiO_x layer grows, but thinner than in the Sc_2O_3 case.

Once the thick sample has been studied, we measure the stoichiometry of the films grown at the different pressures. Figure VI.4 shows the most relevant peaks

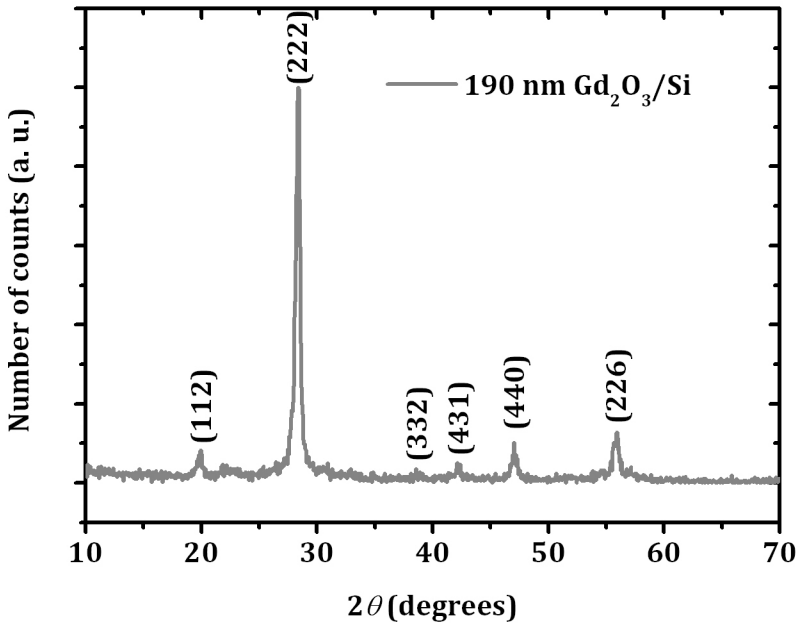

Figure VI.3 GIXRD spectrum of 190 nm Gd_2O_3 on Si. The most relevant peaks of the cubic Gd_2O_3 structure are shown.

in the XPS spectra of the films. The spectra are obtained from the top 2-3 nm of the film. To calculate the chemical composition, we used the peaks at 1187.5 and 531.0 eV. They can be attributed to Gd $d_{5/2}$ and O 1s of the Gd_2O_3, respectively [25], with sensitivity factors of 3.41 and 1.61 [26]. The sensitivity factor of the Gd $d_{5/2}$ was directly measured from a Gd_2O_3 powder sample. The result is that the O/Gd ratio is 1.5 ± 0.1 for all deposition pressures. Then we conclude that, regardless the deposition pressure, the films consisted of stoichiometric Gd_2O_3.

Finally, TEM images of the MIS capacitors with a Ti gate after the FGA at 450 °C are shown in figure VI.5.These TEM samples were prepared from the same devices that were electrically characterized in order to be sure about thicknesses and avoid ambiguities, and thus to obtain an accurate κ value. The Gd_2O_3 films were grown at pressures of (a) 0.50 mbar, (b) 0.75 mbar, (c) 1.0 mbar and (d) 1.3 mbar. First of all, figure VI.5 shows that the gadolinium oxide thickness decreases with the deposition pressure. Since all films were deposited for 30 min, they show a very low deposition rate (below 1 nm/min for pressures larger than 0.75 mbar). Then, an accurate control of the film thickness can be achieved. The decrease of the growth rate with increasing pressure was also observed for ScO_x in

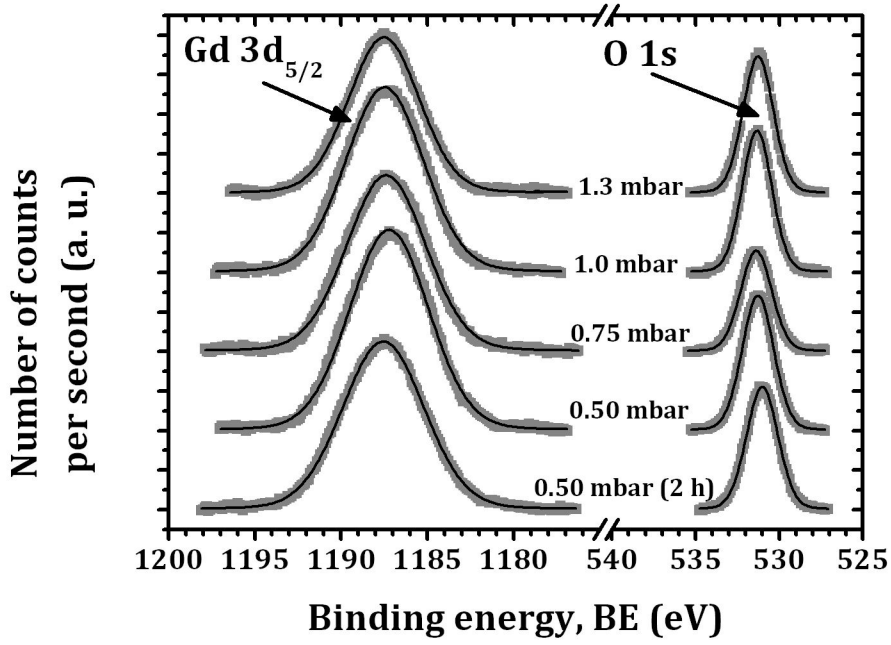

Figure VI.4 XPS spectrum of Gd_2O_3 on Si. The atomic factor of the Gd $3d_{5/2}$ peak is 3.41 and the O 1s peak is 1.61. The atomic ratio [O]/[Gd] is 1.5, then, the oxide is stoichiometric (Gd_2O_3).

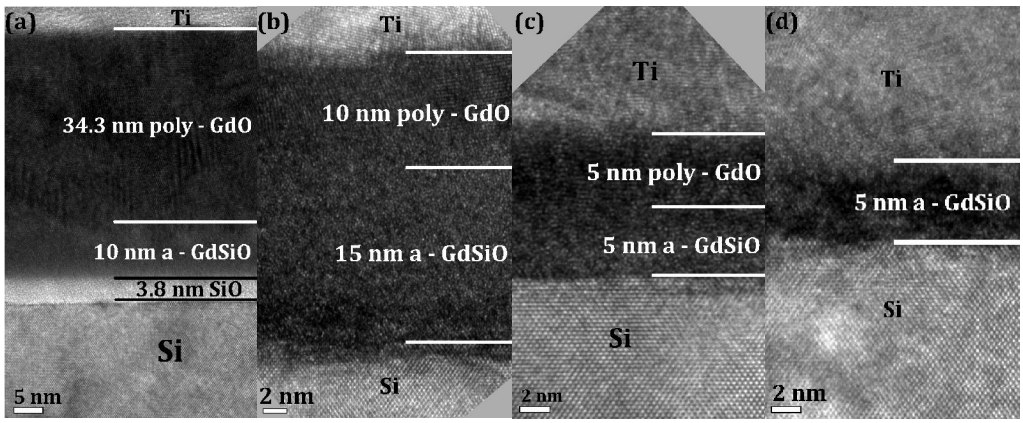

Figure VI.5 TEM images of Ti/GdO/Si MIS devices after FGA at 450 °C. Gadolinium oxide was deposited on Si by HPS at 0.50 mbar (a), 0.75 mbar (b), 1.0 mbar (c) and 1.3 mbar (d) at 40 W for 30 min. No interface SiO_x is observed for pressures above 0.50 mbar due to Ti scavenging. An amorphous gadolinium silicate is formed. For pressures below 1.0 mbar, a poly-crystalline phase is observed.

chapter V and it is caused by a reduction of the rate of the rare earth and oxygen atoms that reach the substrate at higher pressures [27].

In figure VI.5a, the high κ film grown at 0.50 mbar presents a poly-crystalline Gd_2O_3 layer on top of an amorphous gadolinium silicate ($GdSiO_x$). A 3.8 nm SiO_x interfacial layer appears between the $GdSiO_x$ and the Si substrate. The composition of these thin layers was measured by EDX spectrometry during TEM images

acquisition. The presence of an amorphous gadolinium silicate means that gadolinium oxide is reacting with the underlying SiO_2/Si. It cannot be assured if this silicate was formed during deposition or during annealing since there are not TEM images before the FGA. However, XRD did not show any $GdSiO_x$ peaks in the unannealed samples, so this reaction probably happened during the FGA. The instability of Gd_2O_3 against silicate formation on Si substrates has already been reported [28, 29]. This low temperature silicate formation could be interesting for device applications, in order to keep SiO_2-like properties while having Gd_2O_3-like permittivities, as was thoroughly studied in the HfSiON system [30, 31, 32]. The presence of a top poly-Gd_2O_3 agrees with GIXRD results, suggesting that before FGA the sample was poly-crystalline.

For pressures above 0.5 mbar, the interfacial SiO_x seems to be completely scavenged by the Ti gate [33] or dissolved inside the $GdSiO_x$ [34, 35]. Figures VI.5b and VI.5c indicate that for deposition pressures of 0.75 and 1.0 mbar, the dielectric stack also consists of an amorphous $GdSiO_x$ layer under a poly-Gd_2O_3 layer whose thicknesses decrease with deposition pressure. Figure VI.5d shows that for 1.3 mbar, only an amorphous $GdSiO_x$ film is found. This means that the sample was so thin initially that the whole film has become gadolinium silicate. Since no remaining Gd_2O_3 film is found, no information on cristallinity can be obtained, although it is reasonable that, as for the other pressures, the grown film was initially poly-crystalline. Finally, it is important to note that no Ti signal was found by EDX inside the films, indicating that there is no Ti diffusion during FGA.

VI.2.2 Electrical characterization

Figure VI.6 shows C_{HF}-V_G curves of the MIS devices with the thinnest dielectric (the 5 nm dielectric was grown at 1.3 mbar for 30 min). The curves are represented before and after the FGA and for the Pt and Ti gate electrodes. Firstly, it must be noted that before the FGA the capacitance curve is almost identical for both electrodes. This happens in all samples; only Ti and Pt gated MIS devices differ in the sample with the Gd_2O_3 deposited at 0.75 mbar. This indicates a higher thermal budget in this sample during Ti evaporation due to excessive deposition rate. Excluding this sample, the results point to the interpretation that the metal evaporation does not influence the underlying Gd_2O_3. Previous works on plasma

oxidized Gd_2O_3 [36] found that the heating of the sample during Ti evaporation always induces some interface scavenging. However, for Gd_2O_3 samples in this experiment no evaporation-induced scavenging is found. In both cases the thickness of the film is similar, so the difference can be the crystallinity of the films: the plasma oxidized Gd_2O_3 was amorphous while this case presents a poly-crystalline layer. Also the calculated flatband voltages of the curves are similar for both electrodes (0.33 V for Ti and 0.38 V for Pt), where a 1.4 V difference should exist due to the workfunction difference (4.3 eV for Ti and 5.7 eV for Pt [37]). Since the underlying Gd_2O_3 is identical in both cases, this effect can be caused by electrode contamination during evaporation (coming from the crucible, molybdenum for Ti or graphite for Pt) or most likely by dipole formation in the Gd_2O_3/metal interface [38].

In figure VI.6a we observe that the annealing process does not modify the curve when the top metal is Pt, with only a very small variation in flatband voltage (0.38 V for the unannealed, 0.34 V after the FGA). This results from Pt being a noble metal, which should not react with the dielectric. Thus, no changes in the

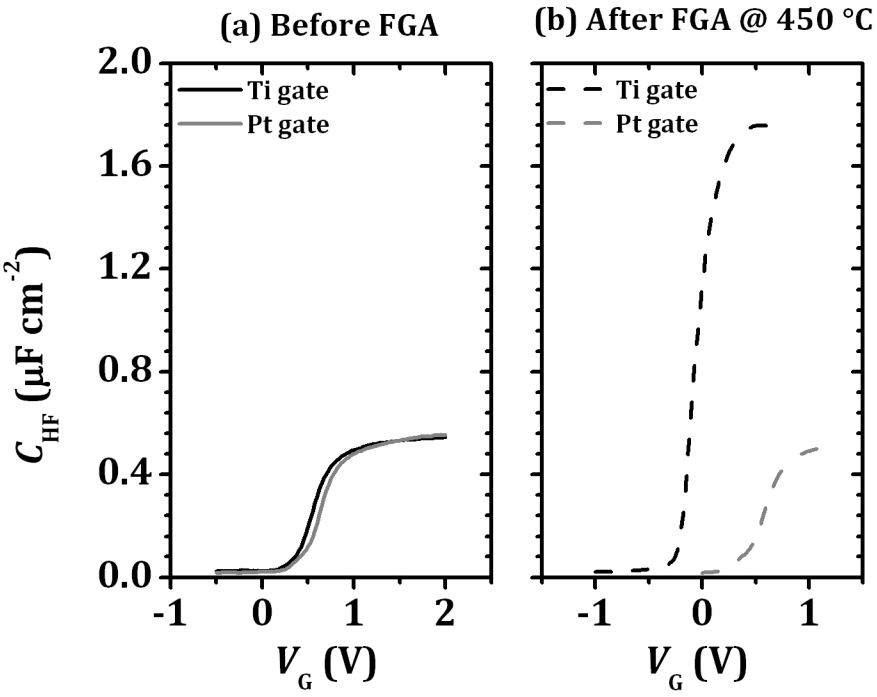

Figure VI.6 C_{HF}-V_G characteristics at 100 kHz for samples before (a) and after (b) the FGA at 450 °C with Ti and Pt gates. For the Pt electrode, the curve does not change significantly after FGA. For the Ti electrode, the capacitance strongly increases due to interface scavenging.

devices are inferred from the C_{HF}-V_G curve. On the other hand, as it can be seen in figure VI.6b, the capacitance in accumulation greatly increases for the Ti gated device after the FGA, going from 0.55 up to 1.8 μF cm^{-2}. The Ti gate is scavenging the SiO_x interface during the FGA, increasing the effective permittivity of the dielectric stack and thus decreasing the equivalent oxide thickness (EOT). In fact, the EOT falls from 6.2 to 1.4 nm in this sample. Also, flatband voltage is shifted towards lower voltages, likely by fixed charges in the dielectric or a dipole change in the Ti/$GdSiO_x$ interface.

The EOTs for all samples are represented in figure VI.7 before (a) and after the FGA at 450 °C (b). Before FGA the EOT of the devices is high, above 5 nm for 1.3 mbar and even higher for the lower deposition pressures. This agrees with the thicknesses of the grown films obtained by TEM, together with the interface SiO_x layer. On the other hand, for all Pt gated devices, the EOT remains with the FGA, while Ti gated devices show a noticeable EOT reduction. As it was seen above, this can be related to the interface scavenging properties of the Ti metal gate. Only the device fabricated at 0.50 mbar does not show this EOT reduction. Since interface scavenging requires oxygen diffusion through the high κ film [39], no scavenging takes place for the thickest layer (in fact, some interfacial regrowth happens as the

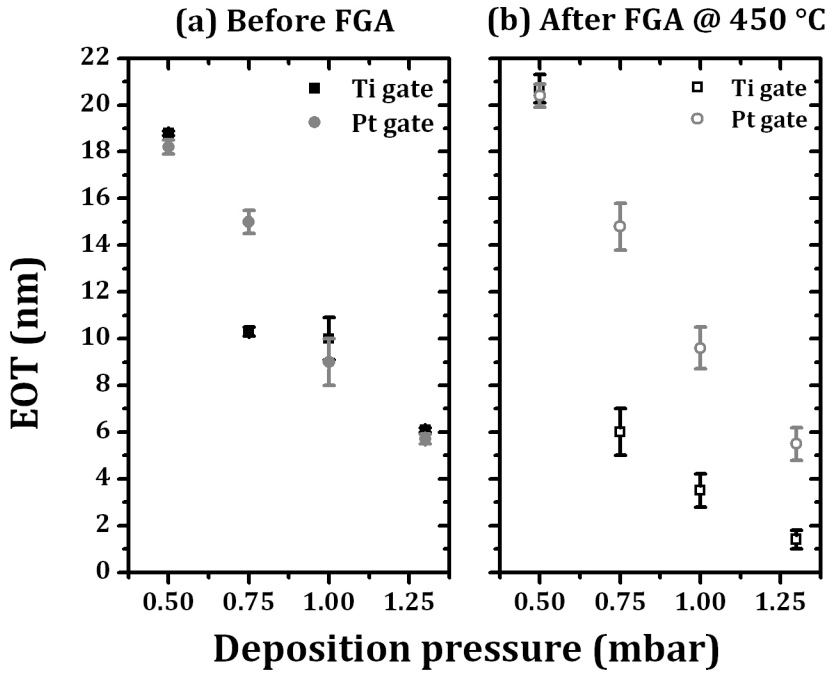

Figure VI.7 EOT as a function of deposition pressure before (a) and after (b) the FGA at 450 °C.

Table VI.1 Deposition pressure, thickness and electrical parameters of the Ti gated MIS devices after the FGA, and effective permittivity of the dielectric stack.

Deposition pressure (mbar)	Dielectric thickness (nm)	Dielectric stack	EOT (nm)	Effective permittivity κ_{eff} (adim.)
0.50	49	$Gd_2O_3/GdSiO_x/SiO_x$	20.7	9
0.75	25	$Gd_2O_3/GdSiO_x$	6.1	16
1.0	10	$Gd_2O_3/GdSiO_x$	3.5	11
1.3	5	$GdSiO_x$	1.4	14

increase in EOT values after FGA show).

The effective permittivity κ_{eff} of the grown films can be calculated from the following equation:

$$\kappa_{eff} = \kappa_{SiO} \frac{t_{dielectric}}{EOT} \qquad \text{equation VI. 1}$$

where κ_{SiO} is the dielectric permittivity of the silicon dioxide (3.9) and $t_{dielectric}$ is the total thickness of the dielectric stack obtained by the TEM images. In this calculation the gadolinium silicate, gadolinium oxide and interfacial SiO_2 are averaged, thus the permittivity is an effective value. However, this is the relevant factor from a device point of view, since even a very high κ value would be compromised for a too thick SiO_x interfacial layer. The table VI.1 presents the results of the Ti gated MIS devices. In spite of the dispersion, we obtained a κ_{eff} above 11 for the samples where the SiO_x interface was completely scavenged. This value is lower than Gd_2O_3 bulk relative permittivity, 14 [3], but this fact is usual for many thin film materials. In this case, the silicate formation observed in TEM likely decreases the effective permittivity. The value obtained for the $GdSiO_x$, the sample deposited at 1.3 mbar, is very close to the bulk Gd_2O_3 value, which suggests that the silicate is Gd rich (in other words, the initial SiO_2 was very thin).

The density of interfacial defects D_{it} before and after the FGA is estimated by the conductance method and is represented as a function of the deposition pressure in figure VI.8. Higher deposition pressures give rise to better quality interfaces, with D_{it} in the order of $1\text{-}2\times10^{10}$ eV^{-1} cm^{-2}. This is a consequence of the lower substrate surface damage during film growth for higher deposition pressures: the species in the plasma reach the substrates by means of a pure diffusion process. Figure VI.8 also shows an unexpected increase of the density of

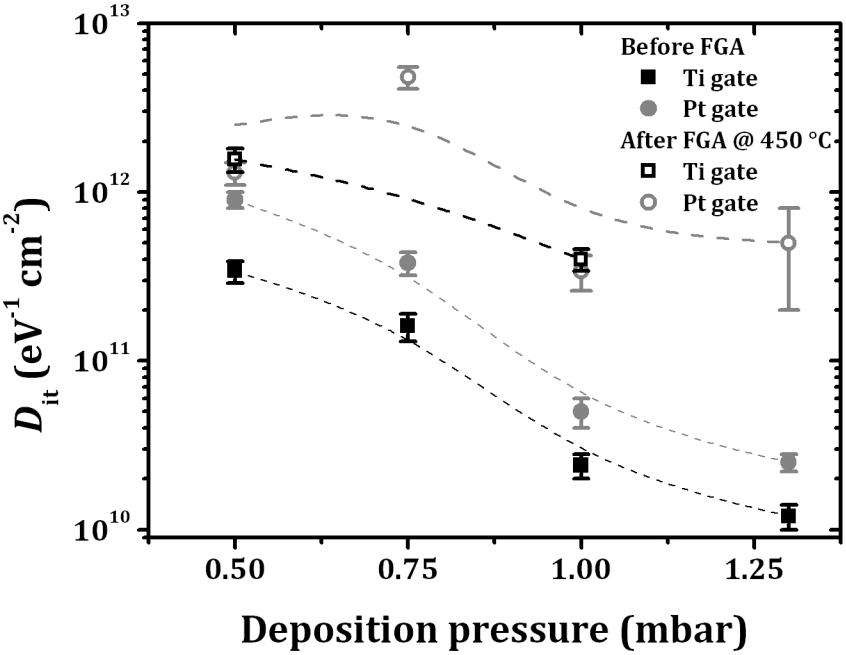

Figure VI.8 Density of interfacial defects D_{it} in function of the deposition pressure estimated by the conductance method. The quality of the interface is increased with the deposition pressure. Lines were drawn as a guide to the eye.

interfacial defects after the FGA, for both Ti and Pt gated devices. For the Ti gated devices, this increase should not be surprising since the scavenging reduces the SiO_x in the interface, increasing the number of defects. However, it also happens for the Pt gated devices, which suggests that the origin is in the silicate formation observed in TEM images. The silicate grows by dissolving the SiO_x layer or even reacting with the Si substrate, which would leave an interface with a higher density of defects. When studying the ScO_x growth in chapter V, the FGA process actually reduced the number of interfacial defects as expected while the silicate formation ($ScSiO_x$) was not observed. This points again to the $GdSiO_x$ formation as the reason for the lower quality of the interface after the FGA.

In addition to this, it is found that only the Gd_2O_3 films grown at 0.50 mbar present a significant hysteresis while films grown at higher pressures do not show any flatband voltage shifts ΔV_{FB}, as can be seen in the C_{HF}-V_G hysteresis curves shown in figure VI.9. The curves were acquired starting in accumulation. This means that for the 0.50 mbar sample there is a positive charge trapping when the device is in inversion. We observed the same ΔV_{FB} behavior as a function of pressure in ScO_x (chapter V), where also the density of defects and the C_{HF}-V_G

hysteresis decreased with the deposition pressure. Then, this confirms the explanation given in there: higher deposition pressures produce thermalization of the plasma species during deposition and thus the dielectric film grows in a less aggressive environment. Therefore, higher deposition pressures mean a lower number of bulk defects and also a lower density of interfacial defects.

VI.3 SUMMARY AND CONCLUSIONS

This chapter demonstrates the viability of producing thin Gd_2O_3 films on Si as high κ dielectric for CMOS applications. It analyzes structural and electrical characterization of Gd_2O_3 grown on Si by HPS for different conditions of pressure. This chapter also studies the influence of the choice of the top electrode metal, comparing Pt (non-reacting) and Ti (interface scavenger).

A thick sample confirmed the growth of the poly-crystalline gadolinium oxide. In thinner high κ films, Gd_2O_3 reacts with the Si substrate and forms an amorphous silicate, probably during the FGA at 450 °C. While the noble metal Pt does not react with the dielectric in the MIS devices, the Ti gate scavenges the SiO_x interfacial layer for thin Gd_2O_3 films, greatly decreasing the EOT of the stack. Higher deposition pressures showed a higher quality in the high κ dielectric/Si

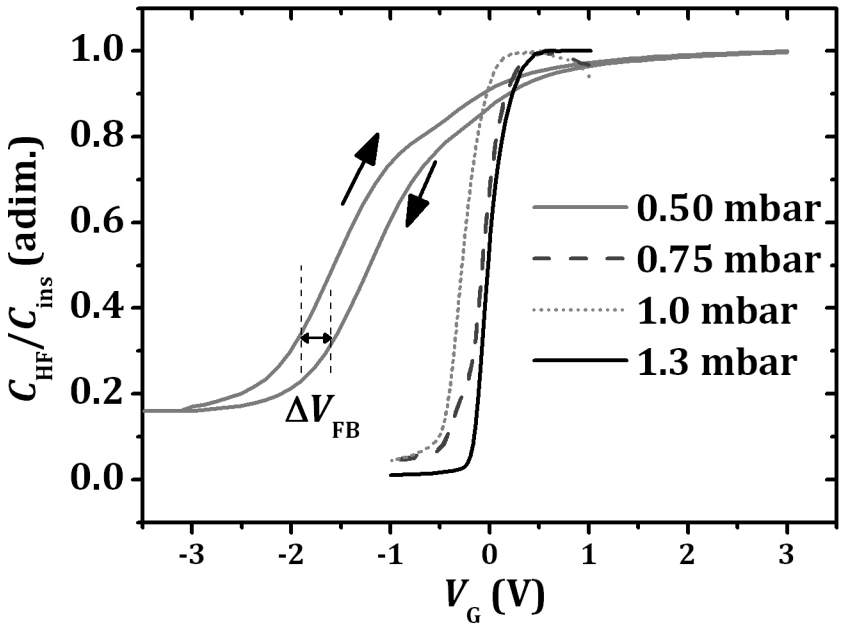

Figure VI.9 C_{HF}-V_G hysteresis curves for Ti/Gd_2O_3/Si stacks, with Gd_2O_3 HPS deposited at several pressures. For pressures above 0.75 mbar, flatband voltage shift ΔV_{FB} is

interfaces with lower densities of defects and hysteresis, although the silicate formation during FGA also degrades the interface quality. An effective permittivity above 11 was calculated for the high κ dielectric stacks. Finally, it is important to note that the gadolinium oxide grown by HPS presents similar electrical trends with deposition pressure than the scandium oxide that was presented in chapter V.

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CHAPTER VII. GADOLINIUM SCANDATE FILMS

In the last years of the 20th century, gadolinium scandate ($GdScO_3$) emerged as a candidate to replace the SiO_2 gate dielectric, due to its high dielectric constant, energy band gap and thermal stability [1, 2, 3]: Haeni *et al*. reported a relative dielectric constant of 20–30 for single crystals depending on the lattice direction [4]; several works determined an optical band gap larger than 5 eV, even for thin films [5, 6, 7]; Zhao *et al*. investigated the thermal stability of $GdScO_3$ [8] and they found that $GdScO_3$ films remain amorphous up to 1000 °C.

So far, $GdScO_3$ thin films have been deposited on silicon by off-axial pulsed layer deposition [8], e-beam evaporation [9], atomic layer deposition (ALD) [10], and liquid injection metal-organic chemical vapor deposition (MOCVD) [11], demonstrating that amorphous $GdScO_3$ films possess a dielectric constant of 22–23. Roeckerath *et al*. fabricated the first metal-insulator-semiconductor field effect transistors (MISFET) with $GdScO_3$ gate oxide on silicon on insulator (SOI) substrates, using a gate last process [12, 13]. They reported a density of interface defects D_{it} of 3×10^{11} eV^{-1} cm^{-2} and a C_{HF} hysteresis of only 50 mV. The leakage current densities remained below 3×10^{-10} A cm^{-2} at 1 V for a 2.2 nm capacitance equivalent thickness (CET). Its suitable properties made this ternary rare earth oxide arise again as a competitor for the next generation of high κ materials, due to the scalability limitations of the Hf-based dielectrics [14] –currently used as gate dielectric.

In this chapter, we demonstrate the gadolinium scandate ($Gd_{2-x}Sc_xO_3$) growth by high pressure sputtering (HPS), which is one of the main objectives of this thesis. Our procedure to grow $Gd_{2-x}Sc_xO_3$ was depositing nano-laminates of scandium oxide and gadolinium oxide (Sc_2O_3 and Gd_2O_3), followed by a FGA (an anneal in *forming gas* atmosphere). This way, we could control the composition of the $Gd_{2-x}Sc_xO_3$ through the thicknesses of the layers of the binary oxides. We evaluated the physical properties of the films by X-ray photoemission spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR), and transmission electron microscopy (TEM). Platinum gated metal-insulator-semiconductor (MIS) devices were fabricated to determine the leakage current, the

high frequency capacitance and conductance (C_{HF}-V_G and G-V_G) curves, the C_{HF} hysteresis and density of interface defects D_{it}. Also, we compare physical and electrical properties of $Gd_{2-x}Sc_xO_3$ to those of its binary constituents.

VII.1 EXPERIMENT

To design the deposition processes of $Gd_{2-x}Sc_xO_3$, we chose Sc_2O_3 and Gd_2O_3 deposition conditions according to the results from chapters IV and V, respectively. There, we concluded that high pressures produce high κ films with lower densities of interfacial defects and lower capacitance hysteresis for both binary materials. Thus, thin layers were grown at a pressure of 1.0 mbar (higher pressures could have prompted instabilities in the plasma, so that the repeatability of the processes would not be ensured). As in the studies of the binary oxides, a radio frequency (*rf*) power of 40 W was used. We tried to control the stoichiometry of the $Gd_{2-x}Sc_xO_3$ layers by using an estimation of the growth rates. We defined the processes to deposit ~6 nm of Sc_2O_3, Gd_2O_3 and Gd-rich $Gd_{2-x}Sc_xO_3$ (with different compositions) from sputtering of the Sc_2O_3 and Gd_2O_3 targets. The Gd-rich $Gd_{2-x}Sc_xO_3$ choice is explained in next section. The ternary oxides were grown by alternating layers of Sc_2O_3 and Gd_2O_3 with thicknesses of less than 0.5 nm. The cycles were repeated from 8 to 12 times.

Plasma was switched on for both targets simultaneously during the whole process, even for the depositions of the binary oxides. However, only one of the targets was on the substrate at a time. In the cases of the binary oxides depositions, one of the plasmas would have sufficed, but we wanted to check if there was contamination from the other target during growth.

Two kinds of substrates were used: high resistivity and low resistivity Si wafers. In the first place, the thin films of high κ materials were deposited on 2-inch double side polished n-Si (100) wafers with a resistivity of 200-1000 Ω cm. These samples were used for physical characterization, and FTIR and XPS spectra were obtained in these samples.

MIS capacitors were fabricated on single side polished 2-inch n-Si (100) wafers, with a resistivity of 1.5-5.0 Ω cm. A 200 nm thick field oxide (SiO_2) was thermally grown to insulate the devices and build up pads (the device contact), as

thoroughly explained in sub-section II.3.2. Square windows with sizes from 10×10 to 700×700 μm^2 were opened on the SiO_2 using a positive photoresist process and immersing the samples in a buffered HF solution. After photoresist removal, samples were cleaned by a standard RCA (*Radio Corporation of America*) process. The wafers were then submerged in a 1:50 HF solution for 30 s to remove the native SiO_2 within the opened windows just before the introduction to the HPS chamber. After high κ dielectric deposition by HPS, the contacts and their pads were defined by a negative photoresist process. Top electrode metals were deposited by e-beam evaporation and lifted off. Finally, a 100 nm Ti/200 nm Al stack was evaporated on the entire back surface of the samples to form the bulk contact.

A 10 nm Pt/70 nm Al stack was used as top electrode in the samples with Sc_2O_3 and Gd_2O_3 as gate dielectrics. The Al capping and the thin Pt layer were motivated by adhesion problems of the Pt on the high κ dielectrics. After optimization of the second lithography step, we evaporated successfully 50 nm Pt layers on the $Gd_{2-x}Sc_xO_3$ films. The noble metal Pt does not react with the high κ material so we could measure the plain properties of three insulators: Sc_2O_3, Gd_2O_3 and Gd-rich $Gd_{2-x}Sc_xO_3$.

We measured high frequency (100 kHz) C_{HF}-V_G and G-V_G curves and the leakage current density (J_G-V_G) at ambient temperature after the fabrication process. Then, the samples were exposed to a FGA at 300 °C and the electrical characterization was repeated. Finally, the characterization was made for the third time after a second FGA at 450 °C. We extracted parameters such as the equivalent oxide thickness (EOT), the flat band voltage (V_{FB}) and the density of interface defects (D_{it}). This way, we analyzed the influence of the FGA on the electrical performance. TEM images were taken from the Pt/$Gd_{2-x}Sc_xO_3$/Si MIS devices after the two anneals. TEM samples were prepared by focused ion beam (FIB).

VII.2 Results and discussion

VII.2.1 Structural characterization

Table VII.1 summarizes the results obtained for the HPS deposition of Sc_2O_3 and Gd_2O_3 at 1.0 mbar, from chapters V and VI. The mean growth rate of Sc_2O_3 and

Table VII.1 Growth parameters of the 1.0 mbar Sc_2O_3 and Gd_2O_3 deposited films.

Target	Deposition time	Pressure	*rf* power	Thickness	Refractive index (adim.)
Sc_2O_3	30 min	1.0 mbar	40 W	6.6±0.2 nm	1.440
Gd_2O_3	30 min	1.0 mbar	40 W	10±1 nm	1.905

Gd_2O_3 are 0.22 and 0.33 nm/min respectively. The obtained refractive index of the Gd_2O_3 lays within the expected range (1.8-2.0) but the Sc_2O_3 film presents a refractive index below the tabulated value (1.8) [15, 16], which could indicate a low Sc_2O_3 density. In chapter VI we also compared FTIR spectra of these binary oxides (figure V.2). We concluded that the Si-O band at around 1050 cm^{-1} is much less intense for the Gd_2O_3. Then Sc_2O_3 produces a SiO_x interface layer much thicker than Gd_2O_3, due to a worse stability in contact with Si. The shift towards lower wavenumbers in the Gd_2O_3 spectrum pointed to the presence of a Si-rich SiO_x or a stressed SiO_2 layer. The following paragraphs demonstrate that, as expected, the thinner films fabricated for this experiment repeat these results.

As it was stated in the previous section, we designed the processes to deposit the ternary rare earth oxide, $Gd_{2-x}Sc_xO_3$, taking into account the growth rates and the FTIR results Sc_2O_3 and Gd_2O_3. We pointed to Gd-rich $Gd_{2-x}Sc_xO_3$ because of two reasons: firstly, FTIR spectra showed that Gd_2O_3 presented a thinner SiO_x interface than Sc_2O_3 and thus it presents a higher stability with Si; secondly, according to reference 17, Gd-rich $Gd_{2-x}Sc_xO_3$ have a higher relative permittivity than other compositions (with a value slightly above 25). In addition, reference 18 concludes that κ values above 20 can be achieved with different cation (Gd or Sc) compositions.

Although we designed deposition processes to obtain $Gd_{2-x}Sc_xO_3$ films with different compositions, its control was more difficult than expected. The hypothesis of linear growth could have led to miscalculations (the initial growth rate could differ from the mean rate). Also, the density of the materials should be taken into account. Anyhow, the most relevant results were obtained for the samples with a composition of $Gd_{1.8}Sc_{0.2}O_3$, for which the subsequent discussion is

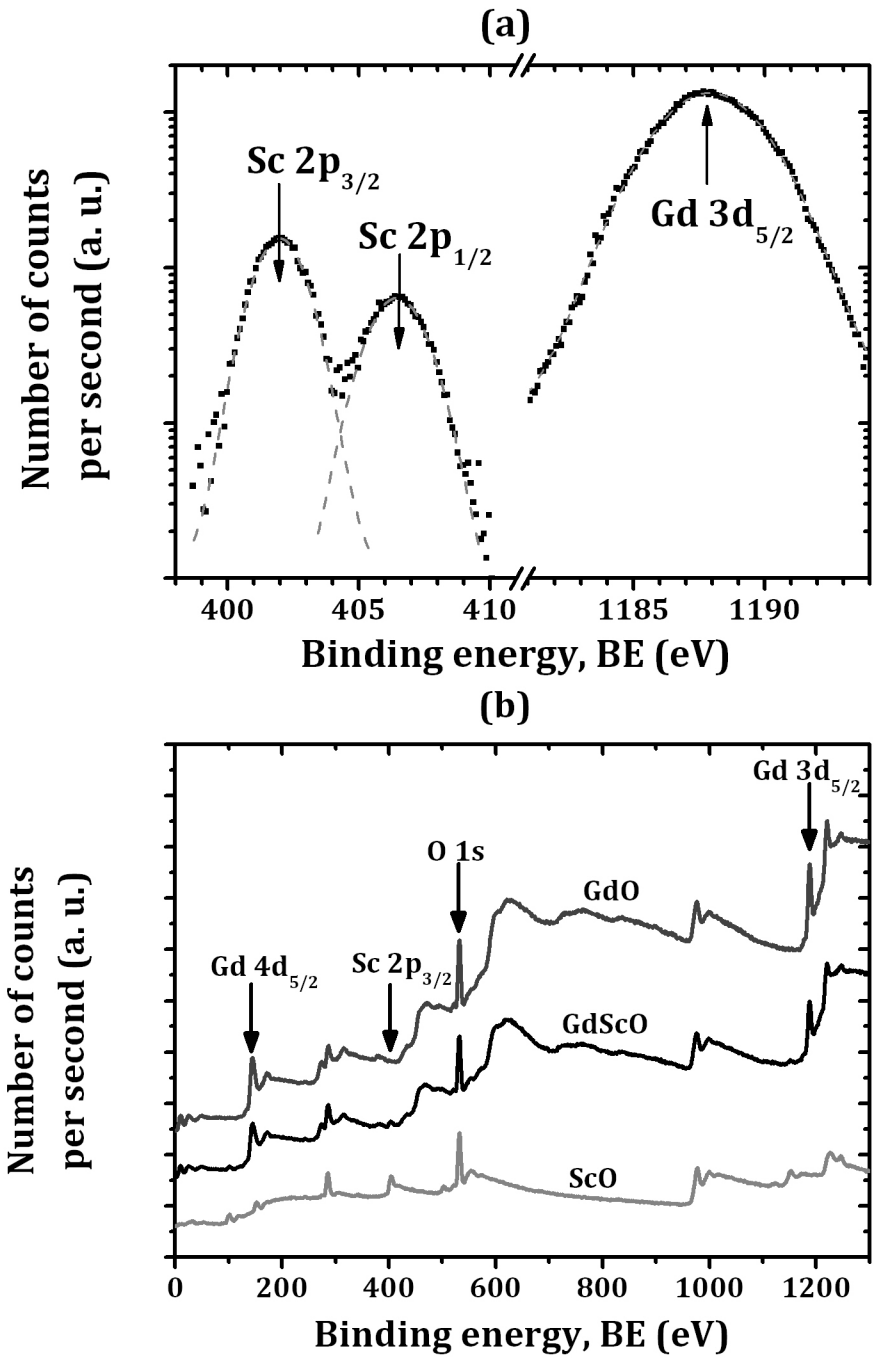

Figure VII.1 (a) Sc 2p and Gd $3d_{5/2}$ XPS peaks of the $Gd_{1.8}Sc_{0.2}O_3$ films. From peak areas and sensibility factors (1.6 for Sc 2p and 3.41 for Gd $3d_{5/2}$), we calculated the composition. (b) XPS spectra of the Sc_2O_3, $Gd_{1.8}Sc_{0.2}O_3$ and Gd_2O_3. Sc_2O_3 spectrum presents no trace of Gd peaks although both targets were switched on during deposition. The same happens for Gd_2O_3.

centered. This stoichiometry was measured by XPS, using the Sc 2p and Gd $3d_{5/2}$ peaks (figure VII.1a). Additionally, the XPS composition measurements from figure VII.1b assure that when a binary Sc_2O_3 or Gd_2O_3 film is grown, it presents no trace of the other material, although both targets were being sputtered during deposition.

Figure VII.2 represents the baseline corrected FTIR spectra of the thin films deposited on Si. They all show a peak at 669 cm^{-1} that corresponds with the C-O bond from the CO_2 in the chamber during measurement. The intensity of the Si-O band at 1025 cm^{-1} indicates again that the Sc_2O_3 produces a thicker SiO_x interface layer than that of the Gd_2O_3. The area of this band is represented for the three high κ materials in the inset of figure VII.2. Regarding the $Gd_{1.8}Sc_{0.2}O_3$ film, it presents a SiO_x film comparable with the Gd_2O_3 interface. Then, the $Gd_{1.8}Sc_{0.2}O_3$ is at least as stable as Gd_2O_3 in contact with Si. The shift of the maximum towards lower wavenumbers indicates again a sub-stoichiometric or stressed SiO_x for the three high κ materials. These spectra exhibit no relevant features below 600 cm^{-1}, where in the previous chapters we found peaks related to Sc-O and Gd-O bonds, most likely because of the small thickness of these films.

To conclude with the structural characterization, figure VII.3 presents a TEM image of a MIS device that consists of a Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si stack after the two FGAs at 300 and 450 °C. This image shows an amorphous dielectric with a thickness of 8±1 nm. Below the dielectric the image shows the typical diffraction patterns of the mono-crystalline Si, while above the dielectric, a poly-crystalline Pt is found. No

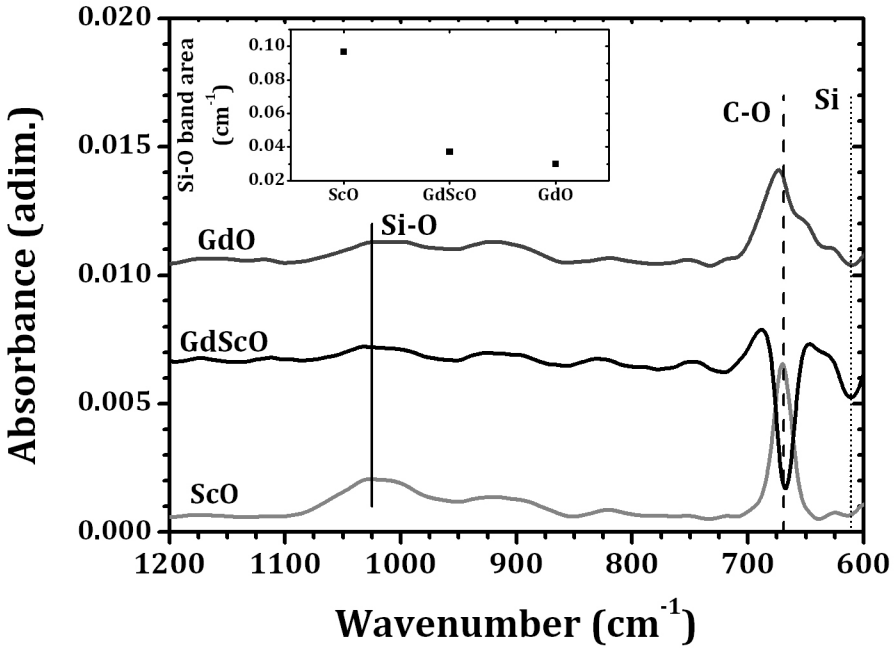

Figure VII.2 FTIR spectra of the Sc_2O_3, Gd_2O_3 and $Gd_{1.8}Sc_{0.2}O_3$ sample films. We corrected substrate absorbance and baseline, and the spectra were shifted vertically for clarity. The inset shows the Si-O band areas for the three films

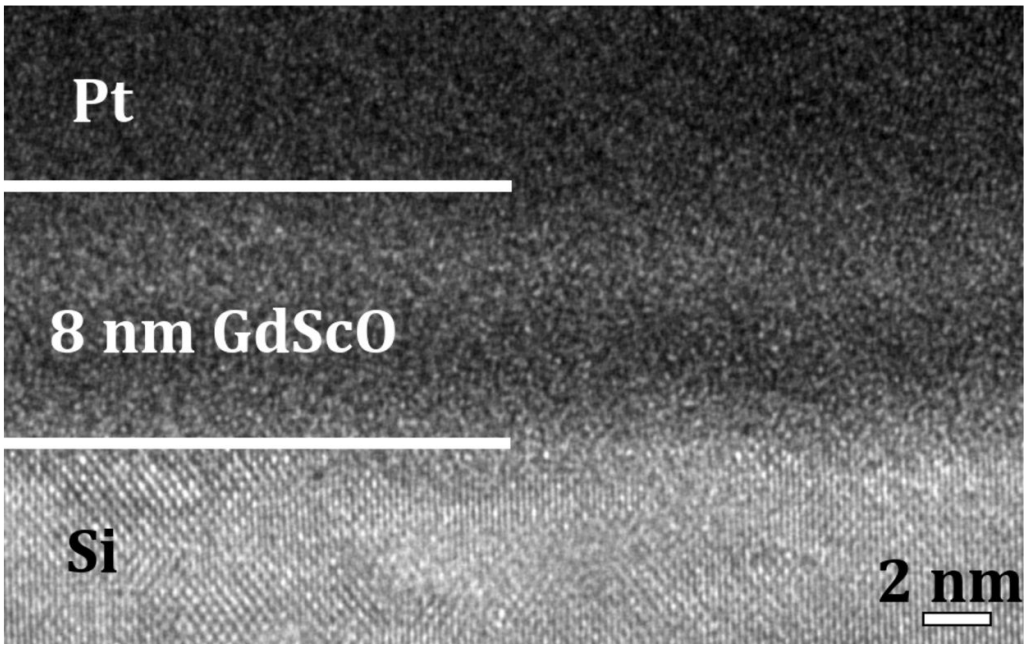

Figure VII.3 TEM image of the Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si MIS capacitor, after the FGA at 300 and 450 °C.

interfacial SiO_x layer between the $Gd_{1.8}Sc_{0.2}O_3$ and the Si substrate is distinguished. Besides, the Pt/$Gd_{1.8}Sc_{0.2}O_3$ interface is also abrupt, as expected, due to the low reactivity of the Pt. Therefore, this result proves that there is no reaction of the high κ dielectric with the substrate or with the metal gate, which could compromise the effective permittivity of the MIS insulator. Then, we can focus future work on scaling the thickness of the ternary layer and thus the EOT of the MIS devices.

Figure VII.4 shows an in-depth sweep in the intensity of energy-dispersive X-ray (EDX) signals, taken during TEM images acquisition. In order to obtain this graph, an electron beam swept the Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si stack and an X-ray detector registered the intensity of a peak of each atom as a function of the position of the beam. This allows the identification of the atoms along the stack. This graph confirms again the presence of $Gd_{1.8}Sc_{0.2}O_3$ as the gate dielectric, sandwiched between the Pt and the Si. Due to the electron spot diameter, we cannot resolve the interfaces sharply. Thus, these curves should not lead to the conclusion of the diffusion of species -if there were diffusion, the spread would be even larger.

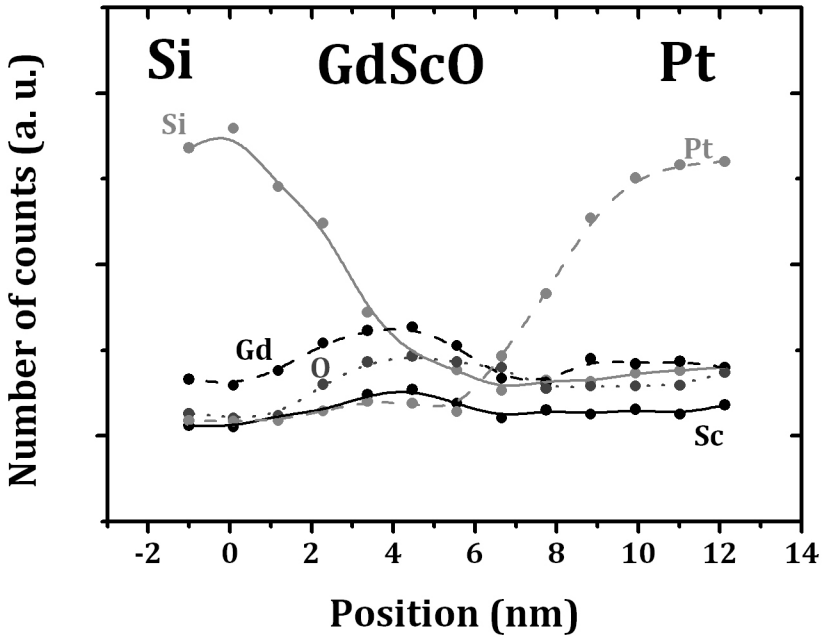

Figure VII.4 Intensity of electron excited X-rays as a function of position in a $Pt/Gd_{1.8}Sc_{0.2}O_3/Si$ MIS capacitor.

VII.2.2 ELECTRICAL CHARACTERIZATION

Figure VII.5 shows the C_{HF}-V_G (a) and G-V_G (b) characteristics of a MIS device with a $Gd_{1.8}Sc_{0.2}O_3$ dielectric unannealed and after the FGA at 300 and 450 °C. The C_{HF} curves indicate that the capacitance measured in accumulation, C_{ins}, increases with the FGA. This means that the dielectric and the substrate do not react to form SiO_x, and thus the $Gd_{1.8}Sc_{0.2}O_3$ is stable in contact with Si. Furthermore, the effective permittivity of the dielectric is increasing, which suggests that the $Gd_{1.8}Sc_{0.2}O_3$ is being formed from its binary constituents with the FGA. The shifts in the V_{FB} indicate that the charge in the dielectric is changing with the FGA.

As we have seen in previous chapters (chapters III, IV, V and VI), the peak in the conductance roughly denotes the density of interfacial defects D_{it}. Although we must extract the influence of the series resistance, the decrease in the peak in the G in figure VII.5b means a lower D_{it} after the FGA and a higher quality of the interface. This is caused by the passivation of the dangling bonds in the dielectric/Si interface with H atoms. We will confirm this result later with the analysis of the calculated D_{it}.

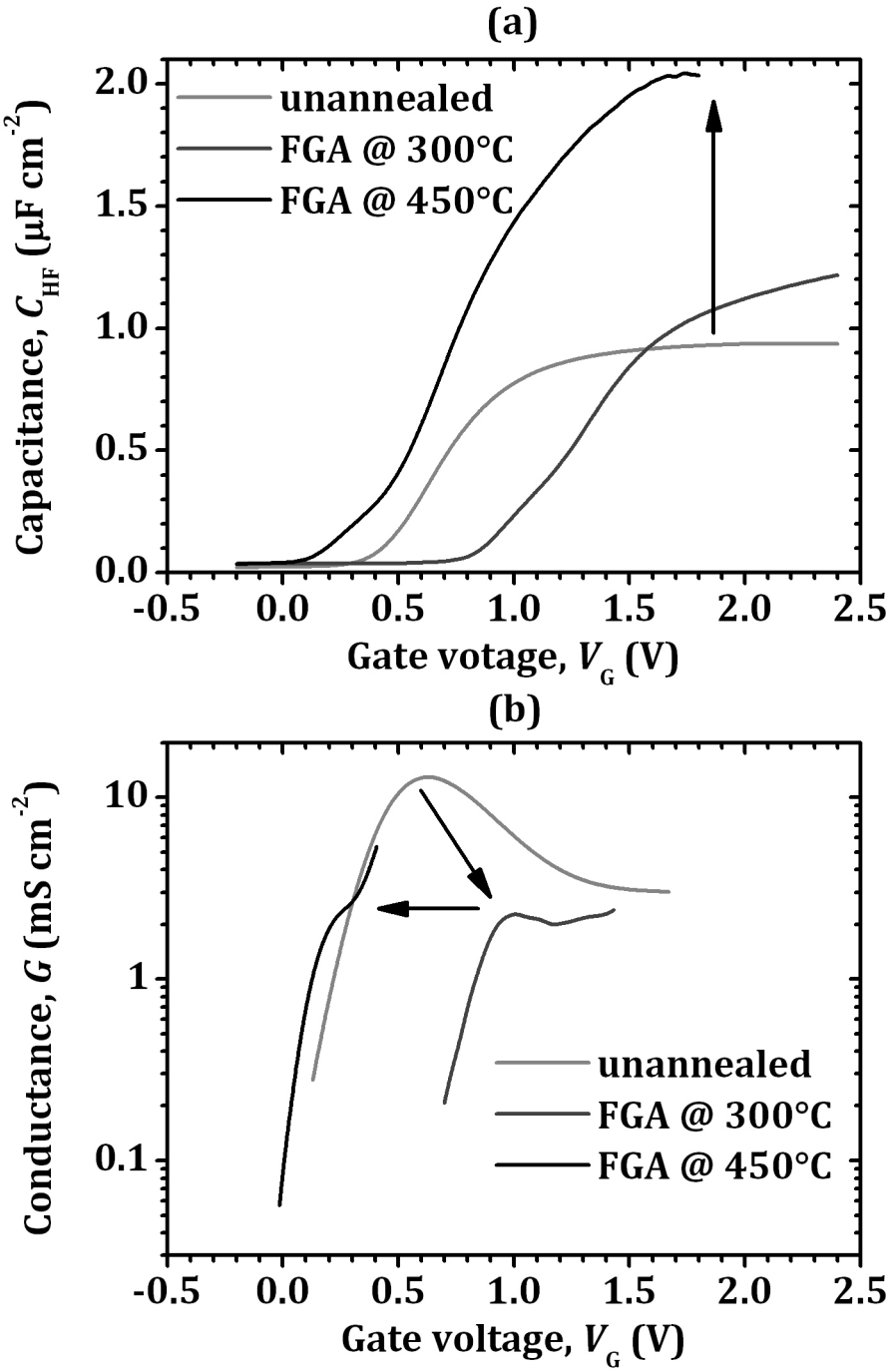

Figure VII.5 (a) C_{HF}-V_G and (b) G-V_G characteristics of the Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si device, after device fabrication, after the FGA at 300 °C and after the FGA at 450 °C.

In summary, the capacitance of the Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si stack increases after the anneals, and thus the FGA reduces the EOT from 3.0 nm to 1.3 nm. As we observe in the TEM image of figure VII.3, the SiO_x does not grow at the dielectric/Si interface. For this film we can calculate a relative dielectric constant of 24, using the measured thickness of 8 nm. Kittl et al. reported a similar value for Gd-rich $Gd_{2-x}Sc_xO_3$ [17]. This relative permittivity lies within the range of 10-30 that is necessary in the next generation of Si device transistors [19], and it is very close to

the value of 25 that would minimize short channel effect in transistors (due to the fringing field in source and drain) [20]. This permittivity confirms $GdScO_3$ as a strong candidate to replace the Hf silicates, whose permittivity is much lower (for $HfSiO_4$, the relative permittivity is around 11) [14]. Besides, the interface traps are partially passivated by the H atoms during the FGA, improving the quality of the interface. In the following paragraphs we compare the electric behavior of the ternary oxide with its binary constituents, Gd_2O_3 and Sc_2O_3.

Figure VII.6 illustrates the evolution of the EOT with the FGA for the Pt gated MIS devices with binary oxides. As we have just pointed out, the EOT of the $Gd_{1.8}Sc_{0.2}O_3$ dramatically decreases with FGA temperature. On the other hand, it increases 0.5 nm for the Gd_2O_3 and 1 nm for the Sc_2O_3. This means that a layer of SiO_x is growing at the dielectric/Si interface for both materials, although the Gd_2O_3 is slightly more stable than Sc_2O_3 in contact with Si. The behavior of the binary oxides is completely opposed to the trend that follows the ternary oxide. This highlights the good stability of $Gd_{1.8}Sc_{0.2}O_3$ and also its higher permittivity as compared to the binary oxides.

The D_{it} values calculated with the conductance method are represented in

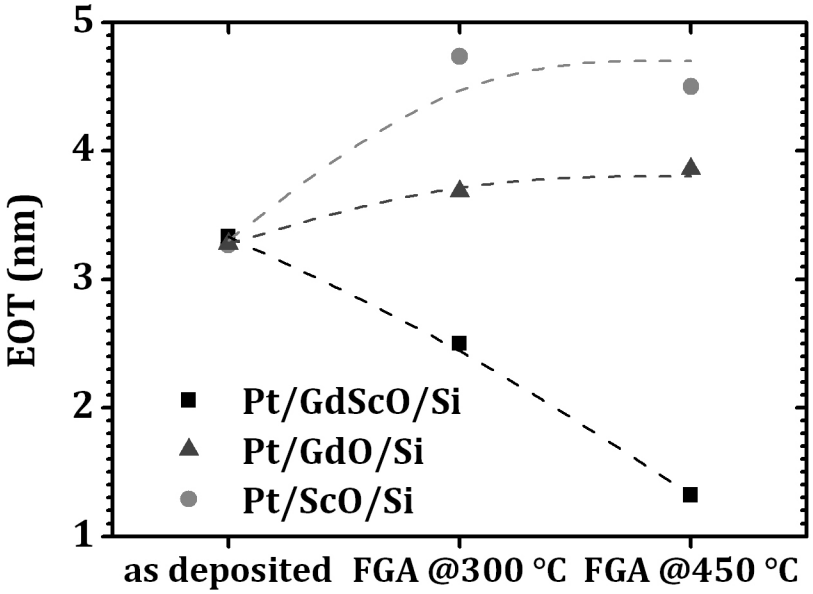

Figure VII.6 Evolution of the EOT with the FGA for the Sc_2O_3, Gd_2O_3 and $Gd_{1.8}Sc_{0.2}O_3$ dielectrics.

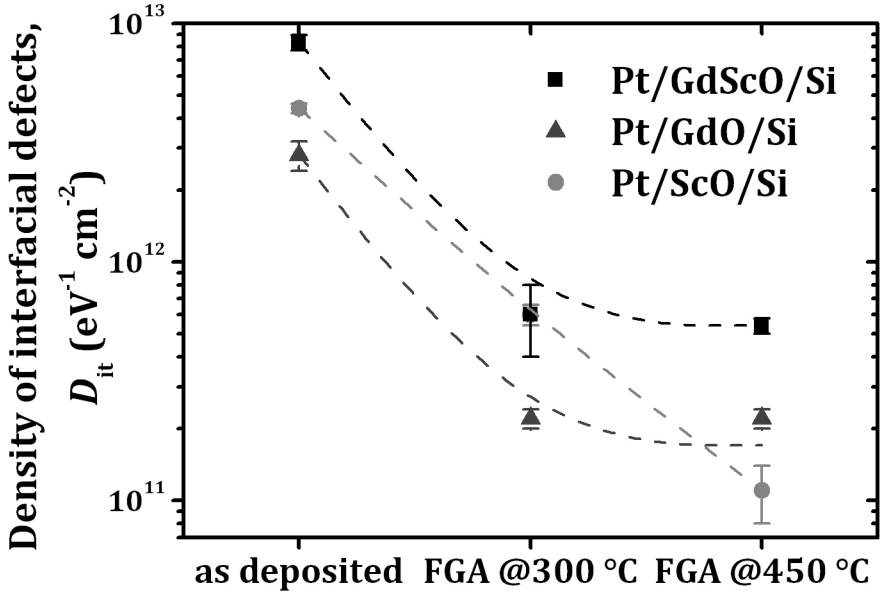

Figure VII.7 Evolution of the D_{it} with the FGA for the Sc_2O_3, Gd_2O_3 and $Gd_{1.8}Sc_{0.2}O_3$ dielectrics.

Figure VII.7 for the unannealed MIS devices and after the FGAs. The passivation of the dangling bonds in the interface makes the D_{it} to decrease for the three high κ materials. For the $Gd_{1.8}Sc_{0.2}O_3$, the passivation effect seems to saturate at 300 °C, improving the D_{it} one order of magnitude compared to the unannealed case and reaching low values of 6×10^{11} eV^{-1} cm^{-2}. The saturation effect also appears for the Gd_2O_3 devices, for which an even lower density of defects is obtained. However, D_{it} is hard to obtain after the second annealing, due to the high conductance in accumulation. Sc_2O_3 presents an even better interface and the saturation is not observed. The higher interface quality of the binary oxides can be related to the regrowth of the SiO_x in the dielectric/Si interface. In fact, a thicker and relaxed SiO_x would also explain the lower D_{it} in the case of the Sc_2O_3.

The C_{HF} hysteresis curves of the Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si devices were determined after the anneals, obtaining a flatband voltage shift ΔV_{FB} of only 55 mV, as can be observed in figure VII.8. This shift is very small compared to the next generation requirements [21, 22], which is another advantage of the ternary rare earth oxide. This low hysteresis must be due to the passivation of the slow response defects during the FGA and a low density of defects in the bulk dielectric.

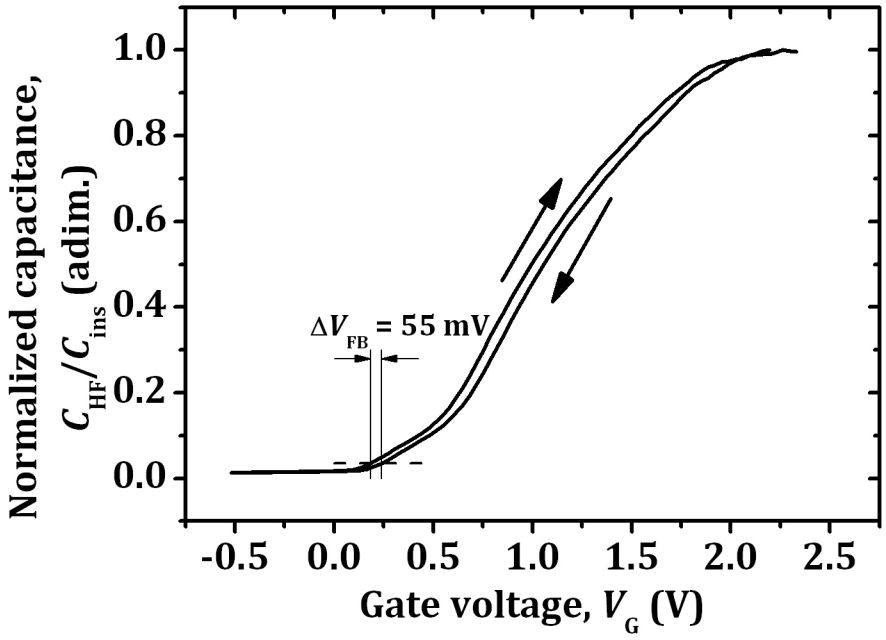

Figure VII.8 C_{HF}-V_G hysteresis curve for the $Gd_{1.8}Sc_{0.2}O_3$ sample. It presents a flatband voltage shift of 55 mV.

Finally, we discuss the leakage current of the MIS devices with the different high κ dielectrics. Figure VII.9a shows the J_G-V_G curves for a Pt/$Gd_{1.8}Sc_{0.2}O_3$/Si stack before and after the anneals. The FGA clearly increases J_G, one order of magnitude after the anneal at 300 °C and about five orders of magnitude after the anneal at 450 °C. Nevertheless, these current densities remain well below the microelectronic industry requirements (around 100 A cm^{-2} for 1 nm EOT at 100 °C [22]). In figure VII.9b we compare the leakage current density at 1 V for the three dielectrics. The Sc_2O_3 presents a higher leakage current than the other two materials before the anneals, but it remains at almost the same value after the FGAs. This can be due to the thick SiO_x interface between the Sc_2O_3 and the Si and its regrowth with the FGAs. On the other hand, the Gd_2O_3 follows the same trend as the $Gd_{1.8}Sc_{0.2}O_3$, but the leakage is lower, which is probably due to a slightly higher Gd_2O_3 thickness, together with the SiO_x interface. In conclusion, the ternary rare earth oxide, despite the low EOT, presents a low leakage current density at 1 V, even after the FGAs.

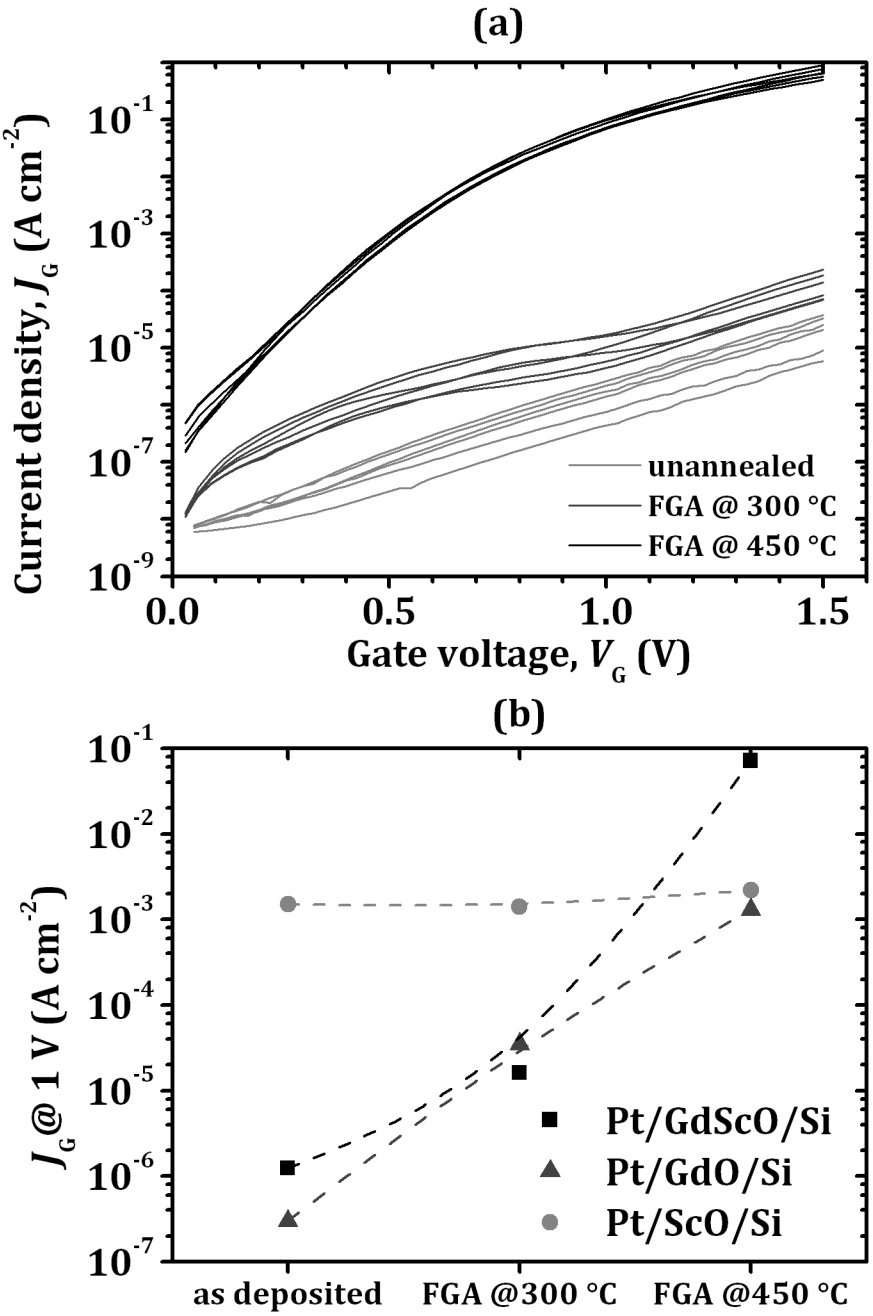

Figure VII.9 (a) J_G-V_G curves of the $Gd_{1.8}Sc_{0.2}O_3$ dielectric before and after the FGA. (b) Evolution of the leakage current density at 1 V for the Sc_2O_3, Gd_2O_3 and $Gd_{1.8}Sc_{0.2}O_3$ dielectrics.

VII.3 Summary and conclusions

In this chapter we have discussed the most relevant results obtained in this thesis: one of the main objectives consisted in depositing gadolinium scandate by HPS from the sputtering of Sc_2O_3 and Gd_2O_3 targets. We explained the design of the processes for the ternary oxide growth on Si and we explored the electrical and

physical characterization of the films, with a thorough comparison with films of the binary oxides.

We measured the composition of the Gd-rich $Gd_{2-x}Sc_xO_3$ by XPS. The most relevant results were obtained from the $Gd_{1.8}Sc_{0.2}O_3$ stoichiometry. The FTIR spectra revealed a very good stability of the ternary oxide after the deposition on Si. MIS capacitors were fabricated to assess the electrical performance of the dielectric. High frequency capacitance measurements showed that FGAs increase the EOT in the case of the binary oxides but in the case of the ternary, the EOT greatly decreases, reaching values of 1.3 nm. The TEM images displayed a 8 nm amorphous $Gd_{1.8}Sc_2O_3$ layer, without any SiO_x interface with the Si. The FGAs passivated the dielectric/Si interfaces, with low densities of defects (below 6×10^{11} eV^{-1} cm^{-2}). The $Pt/Gd_{1.8}Sc_{0.2}O_3/Si$ MIS capacitors also present a small hysteresis after the FGAs and very low leakage currents. Lastly, one of the most relevant results of the present thesis is that we attained an effective relative permittivity of 25, which is an outstanding value for the application of this material in future generations of MISFET devices. In the future we will keep on working with the scalability of this material, aiming at even lower EOTs.

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CHAPTER VIII. ULTRA LOW EOT FINFET RELIABILITY

In chapter I, it was seen that the multi-gate field effect transistors (MuGFETs or FinFETs) are one of the strongest contenders to replace planar CMOS in the near future. They present better short-channel behavior and potential area benefits as compared with their bulk planar counterparts [1, 2, 3]. These advantages, in combination with the small dimensions of the devices, result in higher drive current and lower off currents. Thus, the outcomes of these benefits are better device performance (switching speed) and less power consumption, allowing the continuation of the Moore's law. As it was thoroughly described in chapter II, FinFETs consist of silicon fins which connect source and drain, partially surrounded by the gate stack.

Additionally, to meet the sub-32 nm roadmap requirements, the equivalent oxide thickness (EOT) has to be reduced below 1 nm [4]. Gate stacks based on high κ hafnium dioxide (HfO_2) and TiN as metal electrode are used in order to get these low EOTs, since the TiN gate is known to scavenge the interfacial silicon oxide that unavoidably grows between the silicon and the high κ [5]. The EOT is controlled by the metal gate thickness, which modulates the scavenging effect.

Therefore, the study of the reliability of FinFET devices with EOTs below 1 nm is essential. In this experiment, time dependent dielectric breakdown (TDDB) and positive bias temperature instability (PBTI) are assessed on triple-gate bulk FinFETs with a high κ/TiN gate stack. These two reliability techniques were explained in chapter III. The EOT of the devices ranges from 0.8 to 0.6 nm. This part of the thesis was mainly developed in collaboration with Imec (Leuven, Belgium), thanks to a temporary transfer funded by the Spanish *Ministerio de Educación*.

VIII.1 EXPERIMENT

The FinFET device structure used in this experiment was described in chapter II and shown in figure II.12. In these FinFETs, the silicon fin connects directly with the bulk, and the gate dielectric and metal electrode wrap the top and lateral surfaces of the fin body. The devices were fabricated following the bulk FinFET fabrication flow described in reference 6 and summarized in chapter II.

The main advantage of this triple gated structure is the trade-off between performance and process integration complexity [1, 7], as compared with other FinFET architectures. The main FinFET parameters should be remembered here: the width and the height of the fin, W_{fin} and H_{fin}, respectively; the distance from the gate edge to the source and drain, which is called fin extension, $L_{ext;}$; the number of fins, N_{fin}; and the distance between two adjacent fins or pitch, S.

The n-type FinFETs were fabricated on 300 mm (100) Si wafers. The HfO_2 was deposited by atomic layer deposition (ALD). To minimize EOT, a thin TiN film/poly-Si capping layer gate structure was used to partially scavenge the interfacial layer. The TiN was deposited by physical vapor deposition (PVD). In

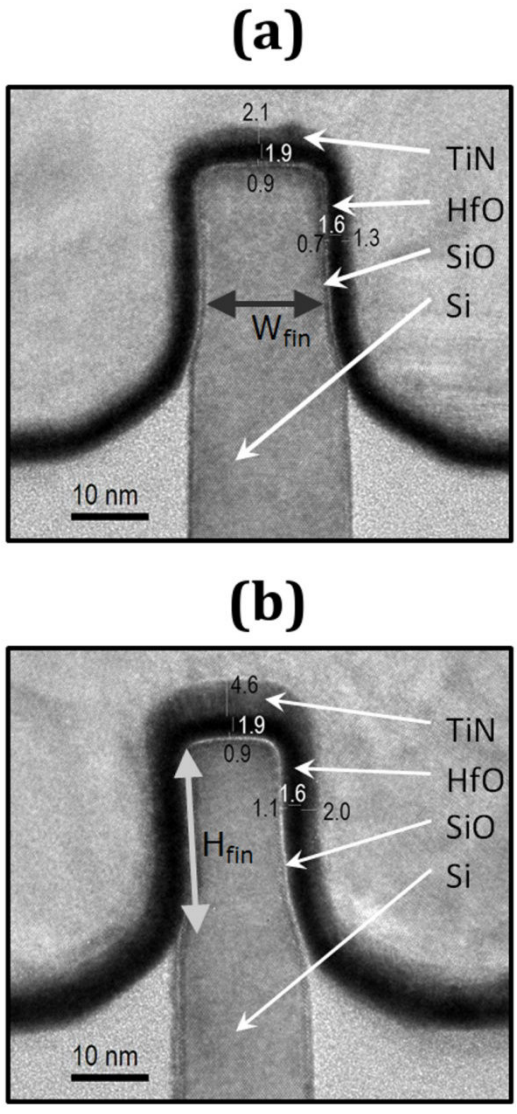

Figure VIII.1 TEM images of FinFETs with TiN/HfO_2 stacks with a (a) 2 nm TiN layer and (b) 5 nm TiN layer

order to achieve gate stacks with different EOT, metal gate thicknesses of 5, 3 and 2 nm were used. Figures VIII.1a and VIII.1b show a transmission electron microscopy (TEM) image of the structure with 5 and 2 nm thick TiN, respectively. The thinner TiN layers reduce more effectively the SiO_x interface layer and this resulted in EOTs of 0.6 nm for the 2 nm TiN, 0.7 nm for the 3 nm TiN and 0.8 nm for the 5 nm TiN.

For TDDB characterization, the N_{fin} is 5 in all cases. Devices with gate lengths L_G of 35 nm and 1 μm were evaluated for comparison. W_{fin}, H_{fin} and S are 20, 27 and 300 nm respectively.

The TDDB test was performed at 125 °C using a constant voltage stress (CVS) where a gate voltage V_G is applied with source, drain and bulk grounded. The gate leakage current is continuously measured during stress. In order to extract the time-to-breakdown (t_{BD}) for each device it is necessary to define a failure criterion, which should distinguish between soft breakdown (SBD) and hard breakdown (HBD), as described in chapter III [8]. Assuming that t_{BD} follows a Weibull distribution, the TDDB data can be fitted to obtain the Weibull slope β and the time to failure of 63% of devices η as a function of V_G, using the Maximum Likelihood Estimation. Considering SBD, for an intrinsic failure distribution, β is related to the number of traps that form a percolation path through the dielectric [9]. As shown in chapter II, the maximum voltage for 10 years lifetime can be extrapolated using a power law model [10], where the acceleration factor is represented by γ. To obtain the lifetime according to the TDDB reliability specification, this extrapolation must be scaled to a gate dielectric area of 0.1 cm^2 and 0.01% failures. For the next generation of electronic devices, the International Technology Roadmap for Semiconductor (ITRS) projects a supply voltage of 0.9 V [4]. Then, it should be assured that transistors operate correctly for 10 years withstanding this voltage.

PBTI was assessed in devices that followed the same fabrication process. N_{fin} in all evaluated devices is 5. L_G, H_{fin} and S are 70 nm, 27 nm and 300 nm respectively, otherwise specified. To distinguish top-wall and sidewall contributions, the number of defects N_{it} was measured by charge pumping for devices with W_{fin} from 20 nm to 1 μm. In order to investigate the possible influence

on PBTI degradation, a H_2 anneal at 800 °C was performed in some devices after fin formation to obtain rounded fin corners [11].

PBTI was performed at 125 °C. Before stress, an I_D-V_G curve was measured to determine the initial threshold voltage $V_{TH,initial}$. Then, a pulse-like voltage stress V_G was applied at the gate, with source, drain and bulk grounded. Between the stress pulses, the gate voltage was switched to $V_{G,sense}$ = $V_{TH,inital}$ and I_D was measured during a few ms, minimizing the delay in order to reduce the V_{TH} recovery effect. The gate voltage overdrive (V_G - V_{TH}) was then extrapolated for 10 years lifetime at 30 mV of V_{TH} shift criterion.

VIII.2 Results and discussion

VIII.2.1 Time-Dependent Dielectric Breakdown (TDDB)

In figure VIII.2, TDDB results for the 0.8 nm EOT FinFET (5 nm TiN) with L_G = 1 μm and W_{fin} = 20 nm are shown. The area of these devices is 3.70×10^{-9} cm^2, which is too large to clearly observe individual SBD paths. The leakage current of around 10 μA is significantly higher compared with the current through single paths created by stress (~10-100 nA) [12] while the creation of multiple parallel paths leads to a progressive increase of the total current or stress induced leakage current (SILC) instead of showing an abrupt increase. Only when one of these SBD paths suffers from wearout, HBD occurs [9] as shown in figure VIII.2a. The time-to-hard breakdown t_{HBD} is obtained using a current step trigger of 10 μA and the Weibull distributions for different gate voltages are represented in figure VIII.2b. The Weibull slope β_{HBD} is 1.53 and in figure VIII.2c the lifetime is extrapolated, obtaining maximum allowable HBD voltage of 1.3 V for 10 years lifetime and an acceleration factor $\gamma$of 56.

If these obtained parameters are compared with the results for planar nMOS devices with similar area and EOT [13], it is found that the values are the same within error (for planar devices, β_{HBD} is 1.54, γ is 47 and the projected allowable voltage is over 1.2 V). This means that the FinFET structure does not introduce new mechanisms of CVS degradation in nMOS. Moreover, leakage current densities are similar for the same stress voltages (10^3 to 5×10^3 A cm^{-2} at V_G = 2.2-2.5 V). One of the major concerns in FinFETs is the concentration of electric field around the

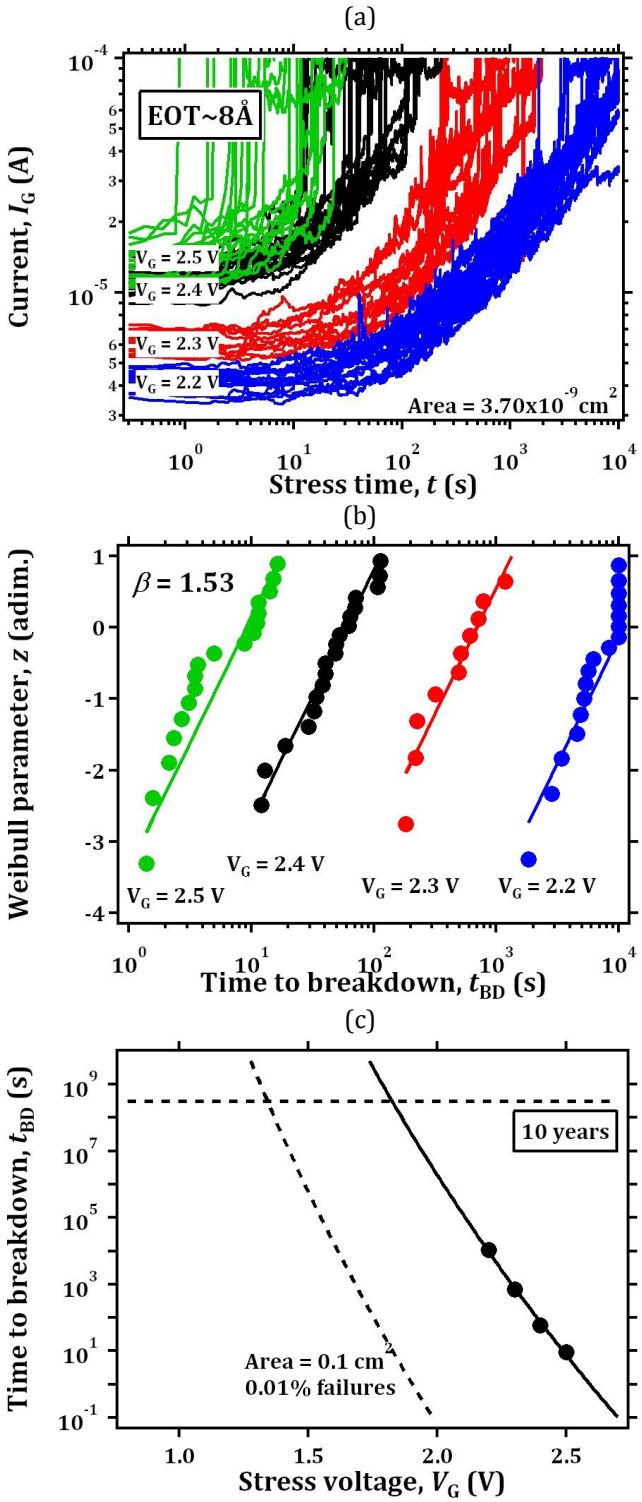

Figure VIII.2 TDDB results for *n*-type devices with EOT~0.8 nm and $A = 3.7\times10^{-9}$ cm^2 stressed at 125 °C. (a) Current traces. (b) Weibull plot. (c) Projected lifetime. Current step for breakdown is 10 μA. Extrapolated operating voltage at a ten-year lifetime is around 1.3 V.

fin-corners, which may induce preferential dielectric breakdown in these regions. Then, the result that nMOS TDDB measurements do not change for FinFET architecture implies that corners do not affect breakdown in this case.

Current-time traces for devices with L_G = 35 nm and W_{fin} = 20 nm (A = 1.30 × 10^{-10} cm^2) are depicted in figure VIII.3. For this smaller area, the gate current and the probability to create a leakage path is lower than in the larger area case. As a consequence, after the beginning of the stress the gate current is constant for a longer time and the creation of a single percolation path is easily recognizable. Thus, SBD can be investigated. Using a current step breakdown trigger of 100 nA, the time-to-soft breakdown (t_{SBD}) is extracted for each device and the statistics are obtained for the different stress voltages. A Weibull slope β_{SBD} of 1.08 -indicating that a path of three traps is necessary to reach SBD [9]- and a γ of 30 are obtained. Since the extrapolated gate voltage at 10 years lifetime is only 0.7 V, as can be seen in figure VIII.4, the target voltage is not met when considering SBD. As with low EOT planar devices, more than 0.01% of transistors would reach the wearout phase at 10 years [8, 12].

Figure VIII.5 represents current traces for devices with A = 3.70×10^{-9} cm^2 (L_G = 1 µm, W_{fin} = 20 nm) and EOT of 0.7 nm (TiN gate thickness of 3 nm). It can be observed that due to the relatively low EOT and the large channel length, the initial leakage current is already high, and the immediate creation of multiple paths

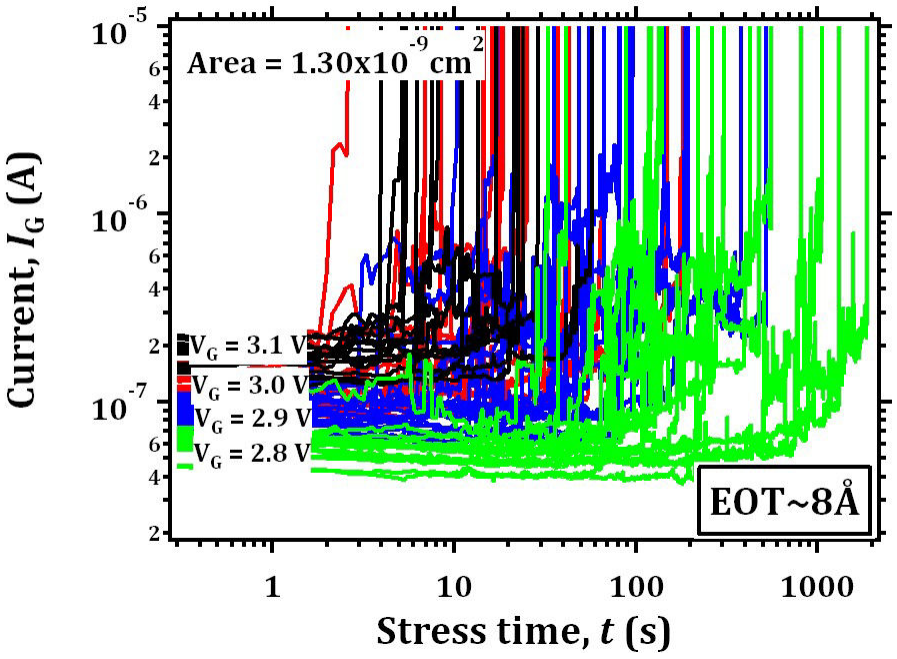

Figure VIII.3 Current traces for *n*-type FinFET devices with 0.8 nm EOT and A = 1.30×10^{-10} cm^2. SBD is evaluated with a current step of 100 nA.

during stress prompts a high SILC. However, before HBD, the leakage current reaches a level where series resistance begins to affect the measurement (typically around 200 μA) [12]. Therefore, not even HBD can be measured in such devices, and for an nMOS TDDB evaluation, only smaller areas can be used.

In figure VIII.6, the current-time traces of the smaller area devices (L_G = 35 nm, A = 1.30×10^{-10} cm^2) with an EOT of 0.7 nm are represented. The gate current is lower and a current step trigger of 200 nA was used to obtain the time-to-soft breakdown t_{SBD}. In this case the Weibull slope is 1.15, indicating again that SBD is formed by a three-trap path through the dielectric. The power law acceleration factor $\gamma$is 32, and the extrapolated voltage at 10 years lifetime is 0.7 V (figure VIII.4). These results are similar to those of the devices with the same area and EOT of 0.8 nm. As observed for devices with 0.8 nm EOT, this extrapolated voltage does not reach the required value for the next generation of transistors. In future work, the wearout has to be included in the TDDB lifetime extrapolation to completely assess the state of the reliability at 10 years.

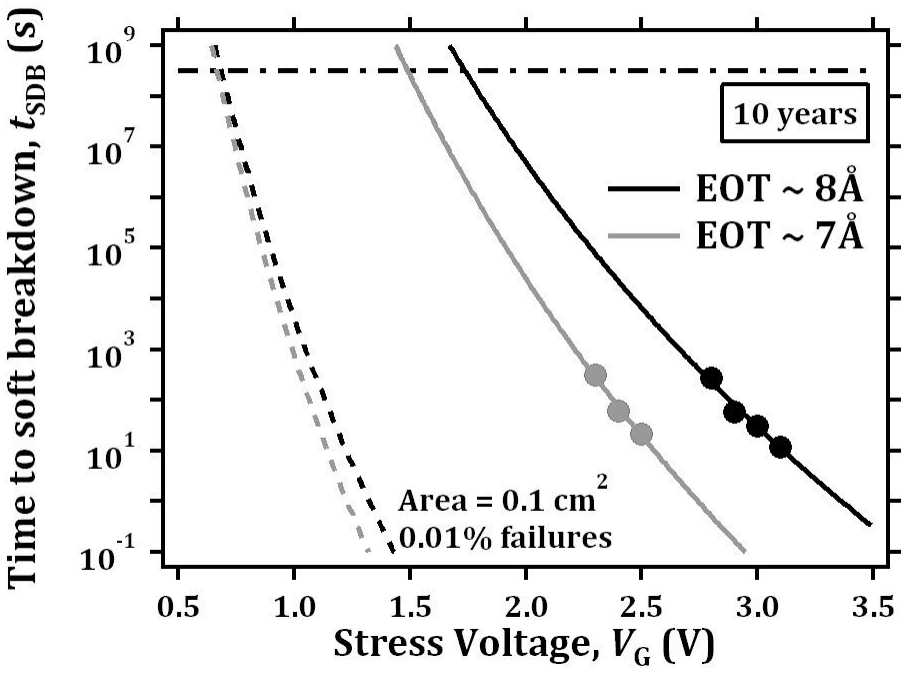

Figure VIII.4 Ten-year lifetime extrapolation for SBD of FinFETs with EOTs of 0.7 and 0.8 nm and A = 1.30×10^{-10} cm^2.

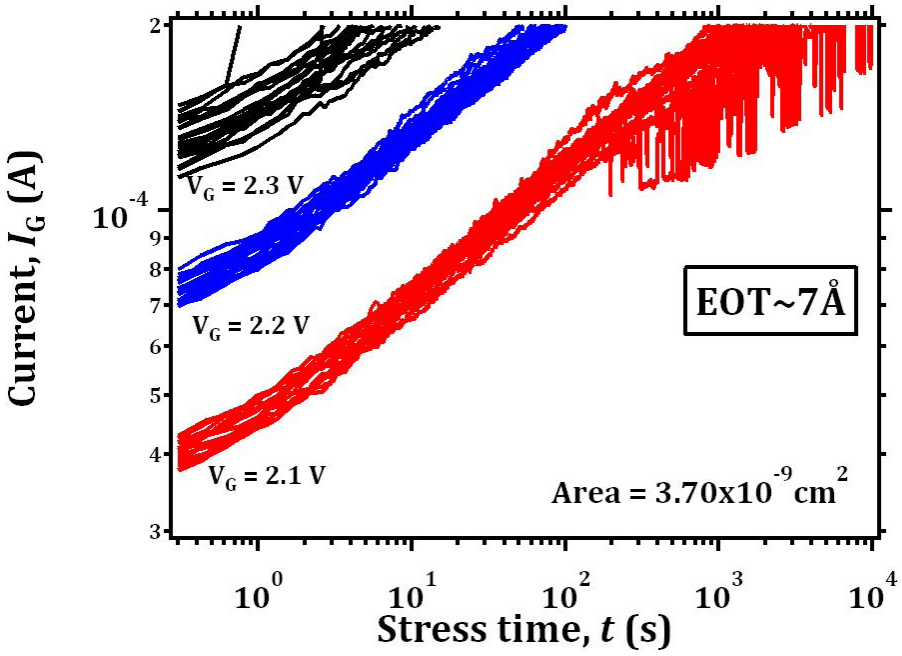

Figure VIII.5 Current-time traces for *n*-type FinFETS devices with 0.7 nm EOT and A = 3.70×10^{-9} cm^2. Current reach series resistance limit before breakdown.

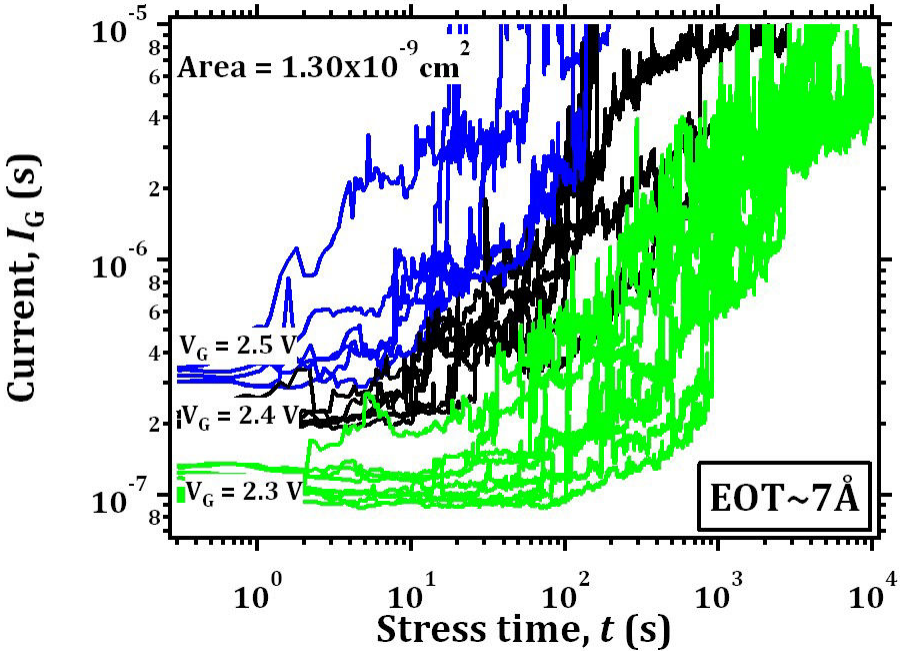

Figure VIII.6 Current-time curves for *n*-type FinFETs with 0.7 nm EOT and A = 1.30×10^{-10} cm^2.

VIII.2.2 Positive Bias Temperature Instabilities (PBTI)

Effect of gate thickness in PBTI

PBTI results for devices with different gate thicknesses are shown in figure VIII.7 for W_{fin} = 20 nm (a), 65 nm (b) and 1 μm (c). For the three dimensions, extracted overdrive at 10 years lifetime decreases drastically with thinner metal gate. As it was shown, EOTs are lower for thinner TiN gates. Then, PBTI degradation for FinFETs is in agreement with the results obtained for planar devices as it is shown in figure VIII.8 [14].

The main mechanism which causes PBTI degradation in devices over 1 nm EOT is known to be electron trapping from the silicon conduction band into defects inside bulk high κ. Then, voltage overdrive at 10 years lifetime improves with thinner EOT because of the lower amount of bulk defects in the high κ to fill. When the SiO_x interlayer is thinner than 1 nm, the potential barrier thickness is reduced and electrons can tunnel even deeper into the high κ. Additionally, it was found that, for sub nanometer EOT planar FET transistors, traps generated during stress near the high κ/Si interface also contribute to V_{TH} shift [13]. The trap generation near the interface may also be affecting in this case, since EOTs below 1 nm are studied. Although lifetimes are slightly better for FinFETs, PBTI seems to be problematic for ultra low EOT devices for both FinFETs and planar devices.

Sidewall and top-wall contributions to PBTI

In figure VIII.9, PBTI degradation is compared for devices with different fin widths. Gate voltage overdrive at 10 years lifetime becomes worse for the wider fin devices. This means that the contribution of the top-wall to the PBTI degradation is larger than the contribution of the sidewalls.

Prior to a deeper investigation, the fin-corner influence on PBTI was checked. In fact, one of the major concerns in FinFETs is the concentration of electric field around the fin-corners, which may induce device degradation focused in these regions. A previous study [15] showed that TDDB improves for devices with rounded corners. Figure VIII.10 shows scanning electron microscopy images of the cross section of a fin (a) before and (b) after the rounding corner process. PBTI results for both devices with and without rounded corners are represented in

figure VIII.11 for W_{fin} of 20 and 65 nm. For the 20 nm W_{fin} devices, corner rounding improves voltage overdrive at 10 years but no effect is observed in wider devices. Hence, sharp corners only affect PBTI when the corner region is large enough in comparison with the channel width. However, this does not explain why large W_{fin} devices present a significantly lower gate voltage over-drive at 10 years.

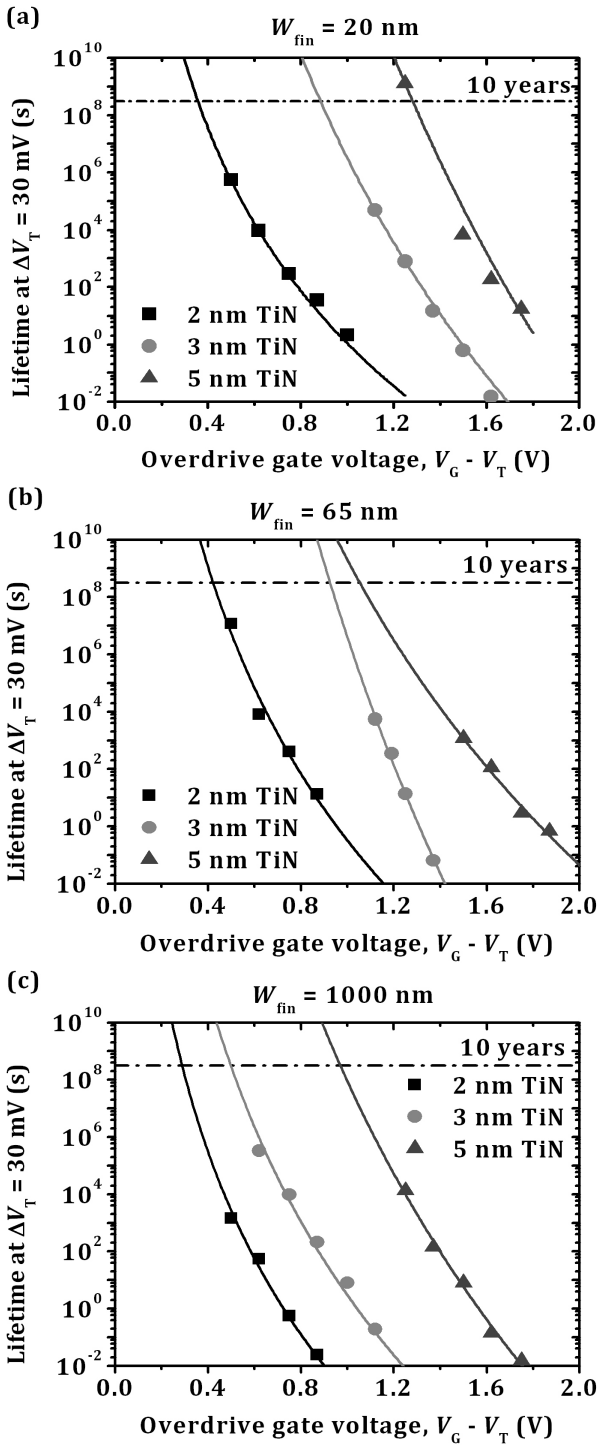

Figure VIII.7 PBTI lifetime versus gate voltage overdrive for different gate thickness for W_{fin} = 20 nm (a), 65 nm (b), and 1000 nm (c).

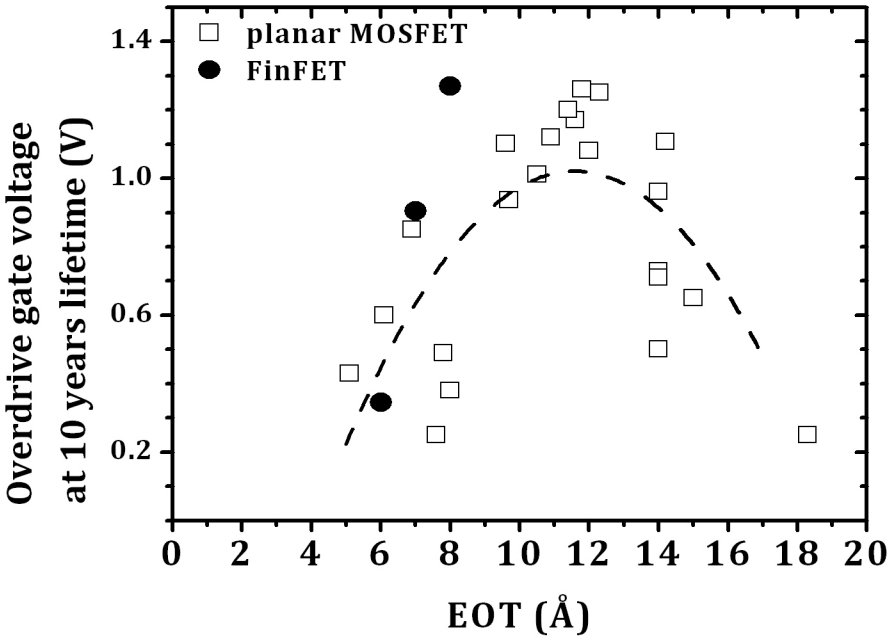

Figure VIII.8 Gate voltage overdrive at ten-year lifetime versus EOT for both planar MOSFETs and FinFETs.

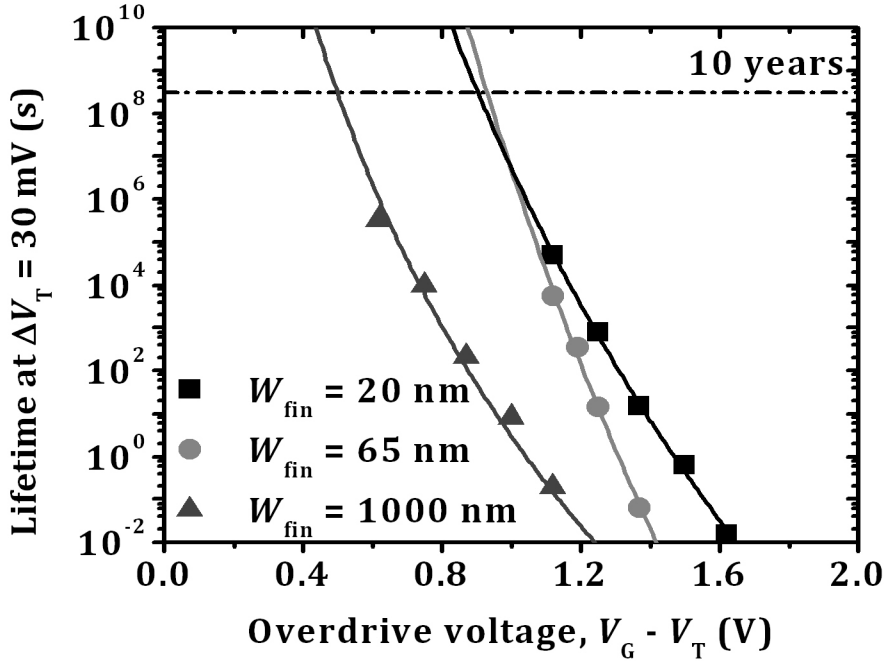

Figure VIII.9 PBTI lifetime versus gate voltage overdrive for different W_{fin} (gate thickness of 3 nm).

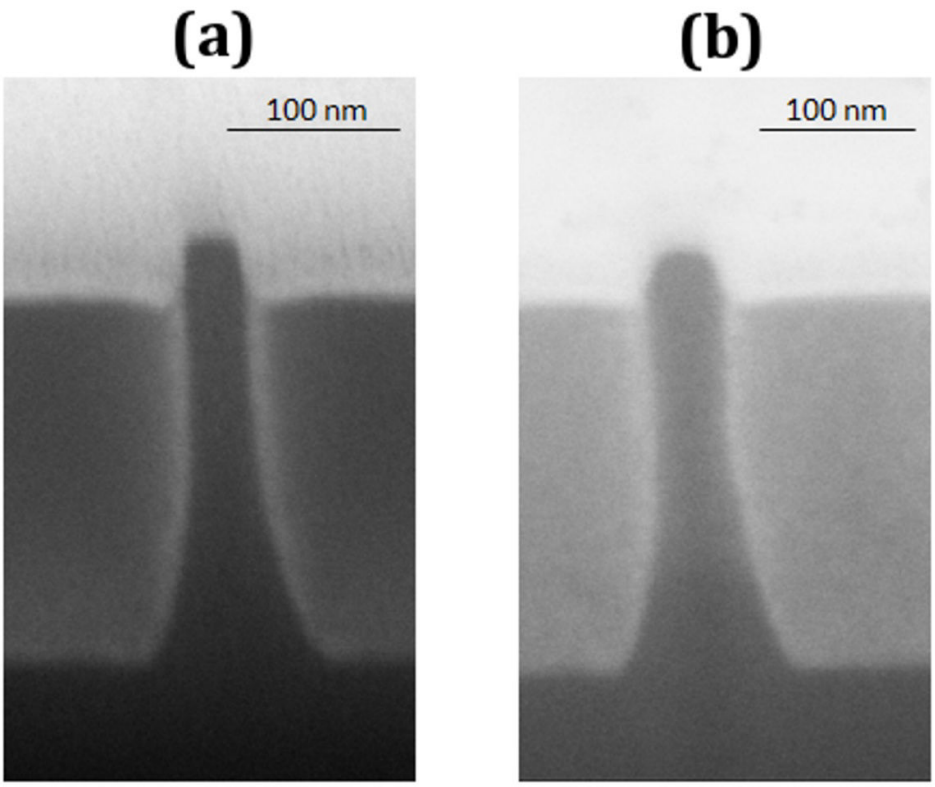

Figure VIII.10 SEM pictures of the fins (a) before the H_2 anneal, showing sharp corners and (b) after the H_2 anneal, showing rounded corners.

A possible explanation for the width effect could be the thinner TiN layer on the sidewalls than on the top-wall, as observed in TEM images (figure VIII.1). Nevertheless, a thinner gate should prompt a higher reduction of the interlayer in the sidewalls than in the top-wall [15]. Then, when top-wall dominated in wide devices with better interface quality, the voltage overdrive at 10 years from PBTI would be higher. However, this is opposite to what is observed in PBTI measurements.

Finally, a higher density of defects in the top-wall high κ dielectric than in the sidewall could be the cause of the increase in degradation. The total number of defects N_{it} was measured by charge pumping at a frequency of 1 MHz in devices with L_G = 10 µm. According to several reports [16, 17, 18], this frequency evaluates the density of defects at 0.5-0.6 nm into the bulk SiO_2 (measured from the Si/SiO_x interface). Since the EOT of the devices is 0.8 nm, we can assume that the measured N_{it} approximately corresponds to the bulk density of defects of the HfO_2 dielectric.

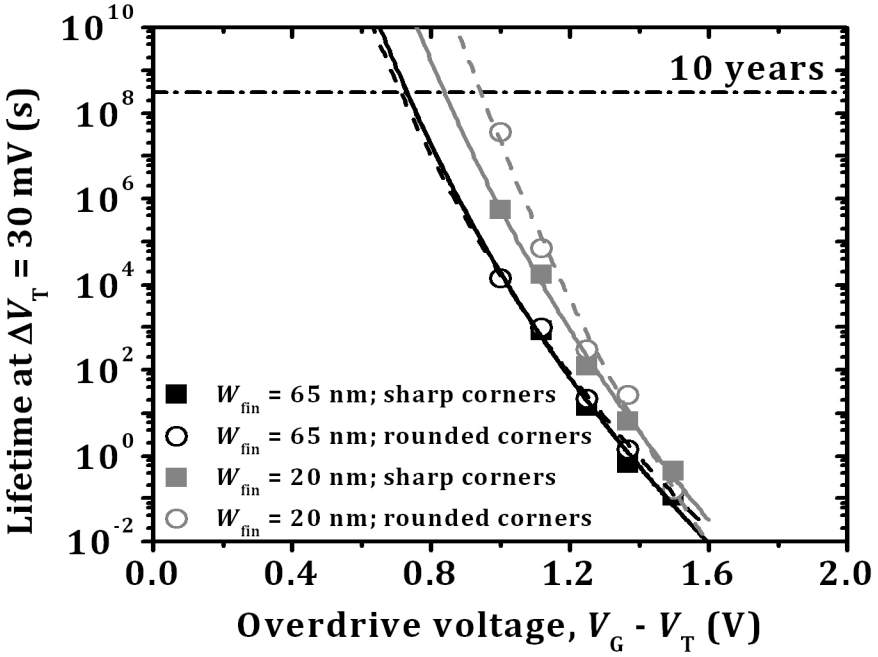

Figure VIII.11 PBTI lifetime versus gate voltage overdrive comparing devices with and without corner rounding for different W_{fin}.

To separate contributions from top-wall and sidewall, N_{it} was determined as a function of fin width [15]. In figure VIII.12, the results of the total number of defects per device are represented as a function of the fin width. These results can be fitted by the following equation:

$$N_{it} = 2H_{fin}L_G N_{fin} N_{it|SW} + L_G N_{fin} N_{it|TW} W_{fin} \qquad \text{equation VIII. 1}$$

where $N_{it|SW}$ and $N_{it|TW}$ are the density of defects in the sidewall and in the top-wall high κ dielectric respectively. It was found that the density of traps in the top-wall (10^{11} cm^{-2}) is larger than the sidewall contribution (2×10^{10} cm^{-2}). This difference is surprising since the crystal orientation of the top-wall is (100) while the one of the sidewalls is (110), which is known to have a higher density of defects [15]. Charge pumping measurements might be distorted by band bending in sub 50 nm W_{fin} devices [19], leading to bad estimation of the density of defects. However, higher $N_{it|TW}$ could have arisen during processing, possibly due to plasma damage caused by PVD of TiN. Whatever the origin, a higher density of traps in bulk high κ dielectric would explain the degraded voltage overdrive at 10 years in wide fin devices.

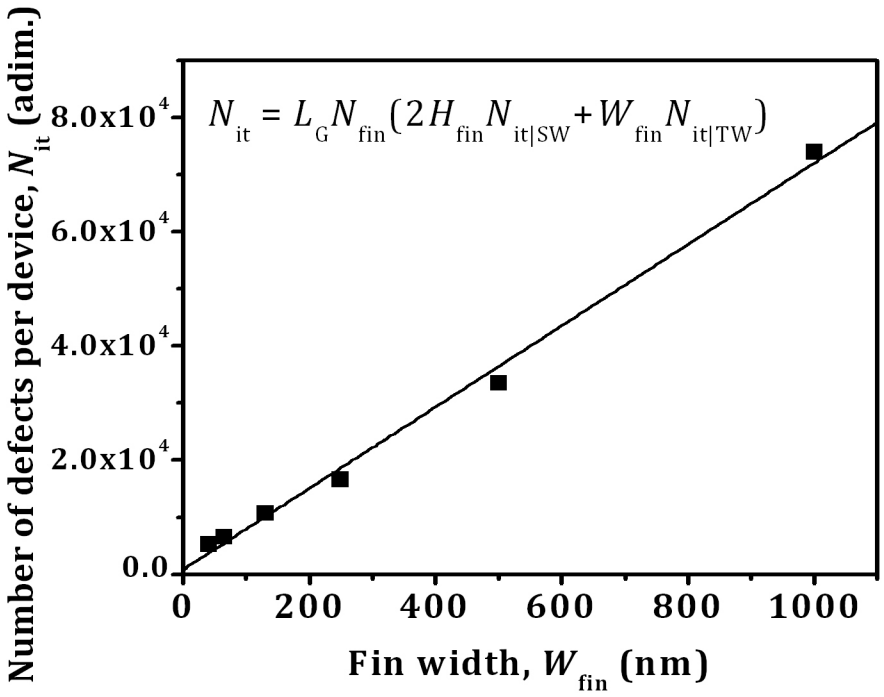

Figure VIII.12 Total density of defects per device versus W_{fin}.

VIII.3 Summary and Conclusions

In this chapter, the reliability of triple gate bulk FinFETs is assessed through the TDDB and PBTI techniques. The gate stack consists of an Hf based high κ dielectric with a TiN metal gate, capped with a poly-Si layer. The EOT of the devices is lower than 1 nm. The influence of these low EOTs is analyzed and the results are compared with planar devices that are provided with the same gate stack.

CVS was applied to n-type bulk FinFETs with sub 1 nm EOT in order to assess the TDDB reliability. It was found that the HBD results for FinFETs with similar area (~10^{-8} cm^2) and EOT (0.8 nm) are analogous to those of the planar devices. This indicates that for this multi gate architecture the breakdown behavior is not affected and no extra degradation mechanism appears in this case. However, for smaller EOT FinFETs, it is very challenging to evaluate TDDB, as it happens with planar devices. This is caused by leakage currents too high to observe SBD, so the series resistance hampers HBD measurements. For smaller channel lengths (and smaller areas) FinFETs, the soft breakdown TDDB reliability can be evaluated. The extrapolated voltages at 10 years lifetime are 0.7 V, which is below the

specifications. To prove sufficient TDDB reliability in future experiments the wearout phase must be taken into account.

PBTI degradation was studied in the same type of devices. Several EOTs below 1 nm (modulated by the TiN gate thicknesses) were compared and it was found that gate voltage overdrive at 10 years lifetime is lower for thinner TiN layer due to the higher reduction of interlayer thickness. Besides, it was observed that fin corner rounding processes could improve PBTI lifetime in narrow devices with 20 nm W_{fin}, due to a lower concentration of electric field in these areas. Finally, a higher density of traps in top-wall high κ oxide could degrade PBTI lifetime in wider fin devices.

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CHAPTER IX. SUMMARY, CONCLUSIONS AND FUTURE WORK

This chapter presents a brief summary of the thesis, the most relevant conclusions from the results and a draft of the new research lines that this work opened and the following experiments that will be carried out.

IX.1 SUMMARY

This thesis has analyzed two approaches to continue with further downscaling of CMOS technology and flash memory devices.

In the first place, we examined three materials for the third generation of high κ dielectrics: Sc_2O_3, Gd_2O_3 and $Gd_{2-x}Sc_xO_3$. They present reported bulk values of permittivity and band gap within the expected range for these microelectronic applications. $Gd_{2-x}Sc_xO_3$ also possesses a great stability in contact with Si and a very high crystallization temperature. We grew the three high κ materials on Si wafers by high pressure sputtering, which is a physical vapor deposition technique that deposits high purity thin films and do not use pollutant gases nor ultra high vacuum. Besides, the use of higher pressures than in conventional sputtering systems produces less substrate damage. The Sc_2O_3/Si interface was analyzed by the use of differently prepared substrates, including native SiO_2, H-terminated Si surface and nitrided Si surface. The properties of Sc_2O_3 and Gd_2O_3 were assessed as a function of the growing conditions (deposition pressure and radio frequency power). The ternary oxide $Gd_{2-x}Sc_xO_3$ deposition was performed by alternation of nano-laminates of its binary components Gd_2O_3 and Sc_2O_3, followed by a post-deposition anneal. Aluminum (reactive), titanium (oxygen solvent or *scavenger*, since it reduces the SiO_2 interface layer) and platinum (non-reacting) metal gates were deposited by e-beam evaporation for MIS devices fabrication to compare the behavior of different metal gates.

On the other hand, we thoroughly study the reliability issues of three dimensional transistor architectures. They are called multiple gate field effect transistors or FinFETs and they are currently replacing traditional planar MISFETs, so the assessment of their reliability becomes vital. Time-dependent dielectric

breakdown and positive bias temperature instabilities were measured in bulk n-type FinFETs with metal/high κ dielectric (TiN/HfO_2) gate stack and an ultra low EOT (below 1 nm).

IX.2 CONCLUSIONS

The main conclusions of the present work are the following.

- We analyzed the Sc_2O_3/Si interface by HPS deposition on Si substrates differently prepared: H-terminated Si, native SiO_2, nitrided Si and deposited SiN_x. Nitrided Si or deposited SiN_x present several advantages over native SiO_2 and bare Si: a higher dielectric constant, the oxygen diffusion avoidance and a higher quality at the dielectric/Si interface. However, since it puts a lower limit on the ultimate achievable EOT, we decided to use H-terminated Si substrates in the following experiments. A relative permittivity of ~9 was found for the Sc_2O_3 films.
- We explored different deposition conditions for ScO_x thin films to evaluate its properties and its interface with Si. Al gated MIS devices were fabricated for electrical characterization. We observed that high deposition pressures (above 1 mbar) reduce interface SiO_x regrowth, increase the quality of the interface and reduce the flatband voltage shift. With this, we showed the advantage of high pressure conditions in reducing the plasma damage to the substrate. The Al gate reacts with the ScO_x, forming an aluminate that degrades the effective permittivity of the high κ dielectric.
- Gd_2O_3 films were deposited on Si with different conditions of pressure. The interface scavenger metal Ti and the non-reacting metal Pt were evaporated for MIS fabrication. While the Pt does not react with the dielectric in the MIS devices, the Ti gate scavenges the SiO_x interfacial layer, greatly decreasing the EOT of the stack. We found, as in the case of ScO_x, that deposition pressures above 1 mbar show lower densities of interface defects, and lower flatband voltage shifts. The Gd_2O_3 films react with the underlying Si and forms a silicate

during the forming gas anneal at 450 °C. This $GdSiO_x$ decreased the effective permittivity of the dielectric stack and thus increased the EOT. An effective relative permittivity of 11 was calculated.

- By alternating the deposition of nano-laminates of Sc_2O_3 and Gd_2O_3 and a post-deposition anneal in forming gas, we grew ~8 nm $Gd_{1.8}Sc_{0.2}O_3$ films. The ternary oxide shows better thermal stability with Si than its binary components, after two anneals at 300 °C and 450° C. Additionally, it maintains the amorphous character. $Pt/Gd_{1.8}Sc_{0.2}O_3/Si$ MIS capacitors were electrically characterized, presenting no observable interface SiO_x, with low density of defects, hysteresis, and leakage currents. A relative permittivity of 25 is found for these devices, which is a great value for the application of this material to the CMOS technology.

- Lastly, we studied reliability of triple gate bulk n-type FinFETs with sub 1 nm EOT through the TDDB and PBTI techniques. TDDB on FinFETs and planar devices are similar for devices with 10^{-8} cm^2 of area, indicating that the breakdown behavior is not affected by the three-dimensional architecture. It is difficult to evaluate TDDB for lower EOTs due to the leakage currents both for FinFETs and planar devices. For smaller areas, the extrapolated voltages at 10 years lifetime are 0.7 V, which is below the specifications.

- Regarding PBTI, gate voltage overdrive (difference between gate voltage and threshold voltage) at 10 years lifetime is lower for thinner EOTs due to the higher reduction of interlayer thickness. Although it is higher than results for planar devices, this value does not meet the requirements for EOT below 0.7 nm. Thus, PBTI can be a problem in the next generations of Si devices. It can be improved by corner rounding processes. A higher density of traps in the top-wall of the fin than in the sidewall was measured, and it degrades PBTI in wider fin devices.

IX.3 FUTURE WORK

Among future experiments, we will design processes for the deposition of gadolinium scandate in order to control its stoichiometry and thickness. We will check the thermal stability and the crystallization temperature of $Gd_{2-x}Sc_xO_3$ in function of the composition and the growing conditions. Also, we must prove the use of thin Ti films as metal gate to further reduce the EOT of $Gd_{2-x}Sc_xO_3$ films by the scavenging effect. We will substitute e-beam evaporation by sputtering deposition for metal gates, with the introduction of new materials such as Ta, TaN and TiN.

We are currently working on deposition of these high κ dielectrics on III-V substrates (InP) and we plan to also use SiGe substrates. Other planned research line is the fabrication of metal insulator metal (MIM) capacitors (or resistive switches) with Sc_2O_3, Gd_2O_3 and $Gd_{2-x}Sc_xO_3$ as high permittivity dielectrics for their application in dynamic random access memories (DRAM) cells.

LIST OF PUBLICATIONS

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1. P.C. Feijoo, A. del Prado, M. Toledano-Luque, E. San Andrés, M.L. Lucía "*Nitridation of Si by N_2 Electron Cyclotron Resonance Plasma and Integration with ScO_x Deposition*," J. of The Electrochem. Soc. 157, H430 (2010).
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